

Evaluation Board User Guide UG-236

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Evaluation Board for the AD5254 Digital Potentiometer

FEATURES

Full featured evaluation board for the AD5254
Several test circuits
Various ac/dc input signals
PC control via a separately purchased system development platform (SDP)
PC control software
12 extra bytes in EEMEM for user-defined information

PACKAGE CONTENTS

Resistor tolerance error stored in EEMEM

EVAL-AD5254SDZ evaluation board
CD that includes
Self-installing software that allows users to control the
board and exercise all functions of the device
Electronic version of the AD5254 data sheet

Electronic version of the UG-236 document

GENERAL DESCRIPTION

This user guide describes the evaluation board for evaluating the AD5254—a quad-channel, 256-position, nonvolatile memory digital potentiometer. With versatile programmability, the AD5254 allows multiple modes of operation, including read/write access in the RDAC and EEMEM registers, increment/decrement of resistance, resistance changes in ±6 dB scales, wiper setting readback, and extra EEMEM for storing user-defined information, such as memory data for other components or a lookup table.

The AD5254 supports a dual-supply ± 2.25 V to ± 2.75 V operation and a single-supply 2.7 V to 5.5 V operation, making the device suited for battery-powered applications and many other applications. In addition, the AD5254 uses a versatile I²C serial interface that operates in fast mode, allowing speeds of up to 400 kbps and supporting the selection of up to four different I²C addresses.

The EVAL-AD5254SDZ can operate in single-supply and dual-supply mode and incorporates an internal power supply from the USB.

Complete specifications for the AD5254 part can be found in the AD5254 data sheet, which is available from Analog Devices, Inc., and should be consulted in conjunction with this user guide when using the evaluation board.

DIGITAL PICTURE OF EVALUATION BOARD WITH SYSTEM DEVELOPMENT PLATFORM

EVAL-AD5254SDZ

Figure 1.

UG-236

Evaluation Board User Guide

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REVISION HISTORY

1/11—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The EVAL-AD5254SDZ supports the use of single and dual power supplies.

In single-supply mode, the evaluation board can be powered either from the SDP port or externally by the J1-1, J1-2, and J1-3 connectors, as described in Table 1.

If dual-supply mode is required, the J1-1, J1-2, and J1-3 connectors must provide the external power supply, as described in Table 1.

All supplies are decoupled to ground using 10 μF tantalum and 0.1 μF ceramic capacitors.

Table 1. Maximum and Minimum Voltages of the Connectors

Connector No.	Label	Voltage	
J1-1	EXT VDD	Analog positive power supply, V _{DD} .	
		For single-supply operation, it is 2.7 V to 5.5 V.	
		For dual-supply operation, it is 2.5 V to 2.75 V.	
J1-2	GND	Analog GND.	
J1-3	EXT VSS	Analog negative power supply, Vss. For single-supply operation, it is 0 V.	
		For dual-supply operation, it is -2.5 V to -2.75 V.	

LINK OPTIONS

Several link and switch options are incorporated in the evaluation board and should be set up before using the board. Table 2 describes the positions of the links to control the evaluation board by a PC, via the SDP board, using the EVAL-AD5254SDZ in single-supply mode. The functions of these link and switch options are described in detail in Table 3 through Table 6.

Table 2. Link Options Setup for SDP Control (Default)

Link No.	Option
A25	3.3 V
A24	GND

Table 3. Link Functions

Link No.	Power Supply	Options			
A25	V _{DD}	This link selects one of the following as the positive power supply:			
		5 V (from SDP).			
		3.3 V (from SDP).			
		EXT VDD (external supply from the J1-1 connector).			
A24 V _{SS} This link selects one of the following as the negative power supply:		This link selects one of the following as the negative power supply:			
		GND (analog ground).			
		VDD VSS (external supply from the J1-3 connector).			

TEST CIRCUITS

The EVAL-AD5254SDZ incorporates several test circuits to evaluate the AD5254 performance.

DAC

RDAC0 can be operated as a digital-to-analog converter (DAC), as shown in Figure 2.

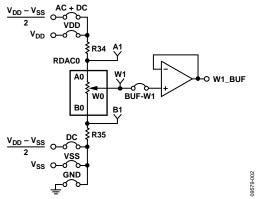


Figure 2. DAC

Table 4 shows the options available for the voltage references.

Table 4. DAC Voltage References

Table 4. DAC voltage References					
Terminal	Link	Options	Description		
A0	A20	AC + DC	Connects Terminal A0 to $(V_{DD} - V_{SS})/2$		
		VDD	Connects Terminal A0 to V _{DD}		
W0	BUF-W1		Connects Terminal W0 to an output buffer		
В0	A21	DC	Connects Terminal B0 to (V _{DD} – V _{SS})/2		
		VSS	Connects Terminal B0 to Vss		
		GND	Connects Terminal B0 to analog ground		

The output voltage is defined in Equation 1.

$$V_{OUT} = (V_{A0} - V_{B0}) \times \frac{RDAC0}{256}$$
 (1)

where:

RDAC0 is the code loaded in the RDAC0 register. V_{A0} is the voltage applied to the A0 terminal (A20 link). V_{B0} is the voltage applied to the B0 terminal (A21 link).

Using the R34 and R35 external resistors, you can reduce the voltage of the voltage references. In this case, use the A1 and B1 test points to measure the voltage applied to the A0 and B0 terminals and recalculate V_{A0} and V_{B0} in Equation 1.

AC Signal Attenuation

RDAC0 can be used to attenuate an ac signal, which must be provided externally using the AC_INPUT connector, as shown in Figure 3.

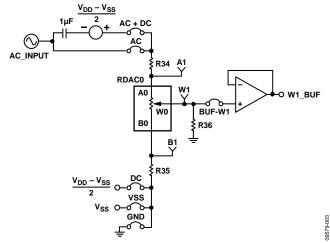


Figure 3. AC Signal Attenuator

Depending on the voltage supply rails and the dc offset voltage of the ac signal, various configurations can be used, as described in Table 5.

Table 5. AC Signal Attenuation Link Options

Voltage	Maximum AC Signal		•	
Supply	Amplitude	Link	Options	Conditions
Single	V_{DD}	A20	AC + DC	No dc offset voltage
				AC signal is outside the voltage supply rails due to the dc offset voltage
				DC offset voltage ≠V _{DD} /2 ¹
			AC	All other conditions
		A21	DC	Use in conjunction with AC + DC link
			GND	All other conditions
Dual	V _{DD} /V _{SS}	A20	AC + DC	AC signal is outside the voltage supply rails due to the dc offset voltage
				DC offset voltage ≠0 V¹
			AC	All other conditions
		A21	GND	Use in conjunction with AC + DC link
			VSS	All other conditions

 $^{^{\}rm 1}$ Recommended to ensure optimal total harmonic distortion (THD) performance.

The signal attenuation is defined in Equation 2.

$$Attenuation (dB) = 20 \times \log \left(\frac{R_{WB0} + R_W}{R_{END-TO-END}} \right)$$
 (2)

where:

 R_{WB0} is the resistor between the W0 and B0 terminals. R_W is the wiper resistance.

 $R_{END-TO-END}$ is the end-to-end resistance value.

In addition, R36 can be used to achieve a pseudologarithmic attenuation. To do so, adjust the R36 resistor until a desirable transfer function is found.

Signal Amplifier

RDAC1 can be operated as an inverting or noninverting signal amplifier supporting linear or pseudologarithmic gains. Table 6 shows the available configurations.

Table 6. Amplifier Selection Link Options

Amplifier	Gain	Link	Label
Noninverting	Linear	A27	LINEAR
		A29	NON-INVERTING
		A30	NON- INVERTING
	Pseudologarithmic	A27	PSEUDOLOG
		A29	NON- INVERTING
		A30	NON- INVERTING
Inverting	Linear	A27	LINEAR
		A29	INVERTING
		A30	INVERTING
	Pseudologarithmic	A27	PSEUDOLOG
		A29	INVERTING
		A30	INVERTING

The noninverting amplifier with linear gain is shown in Figure 4, and the gain is defined in Equation 3.

$$G = 1 + \frac{R_{WB1}}{R38} \tag{3}$$

where R_{WB1} is the resistor between the W1 and B1 terminals.

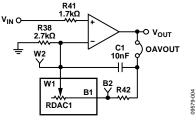


Figure 4. Linear Noninverting Amplifier

The noninverting amplifier with pseudologarithmic gain is shown in Figure 5, and the gain is defined in Equation 4.

$$G = 1 + \frac{R_{WBI}}{R_{AWI}} \tag{4}$$

where:

 R_{WB1} is the resistor between the W1 and B1 terminals. R_{AW1} is the resistor between the A1 and W1 terminals.

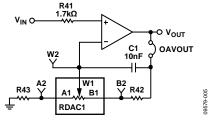


Figure 5. Pseudologarithmic Noninverting Amplifier

R43 and R42 can be used to set the maximum and minimum gain limits.

The inverting amplifier with linear gain is shown in Figure 6, and the gain is defined in Equation 5.

$$G = -\frac{R_{WBI}}{R38} \tag{5}$$

where R_{WB1} is the resistor between the W1 and B1 terminals.

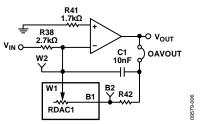


Figure 6. Linear Inverting Amplifier

The inverting amplifier with pseudologarithmic gain is shown in Figure 7, and the gain is defined in Equation 6.

$$G = -\frac{R_{WBI}}{R_{AWI}} \tag{6}$$

where:

 R_{WB1} is the resistor between the W1 and B1 terminals. R_{AW1} is the resistor between the A1 and W1 terminals.

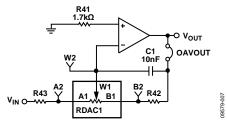


Figure 7. Pseudologarithmic Inverting Amplifier

R43 and R42 can be used to set the maximum and minimum gain limits.

Output Buffers

RDAC2 and RDAC3 can be connected to an output buffer as shown Figure 8 and Figure 9.

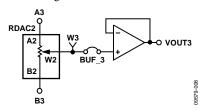


Figure 8. RDAC2

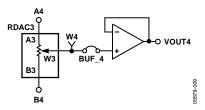


Figure 9. RDAC3

EVALUATION BOARD SOFTWARE

INSTALLING THE SOFTWARE

The EVAL-AD5254SDZ evaluation kit includes evaluation board software provided on a CD. The software is compatible with Windows* XP, Windows Vista, and Windows 7 (both 32 and 64 bits).

Install the software before connecting the SDP board to the USB port of the PC to ensure that the SDP board is recognized when it is connected to the PC.

- 1. Start the Windows operating system and insert the CD.
- 2. The installation software must open automatically. If it does not, run the **setup.exe** file from the CD.
- 3. After installation is completed, power up the evaluation board as described in the Power Supplies section.
- 4. Plug the EVAL-AD5254SDZ into the SDP board and the SDP board into the PC using the USB cable included in the box.
- 5. When the software detects the evaluation board, follow the instructions that appear to finalize the installation.

To uninstall the program, click **Start > Control Panel > Add or Remove Programs > AD5254 Eval Board.**

RUNNING THE SOFTWARE

To run the evaluation board software, do the following:

- Click Start > All Programs > Analog Devices > AD5254
 > AD5254 Eval Board.
- If the SDP board is not connected to the USB port when the software is launched, a connectivity error is displayed (see Figure 10). Connect the evaluation board to the USB port of the PC, wait a few seconds, click **Rescan**, and follow the instructions.



Figure 10. Pop-Up Window Error

The main window of the EVAL-AD5254SDZ evaluation software then opens, as shown in Figure 11.

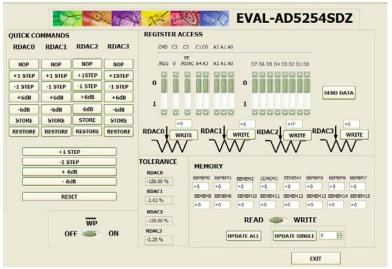


Figure 11. EVAL-AD5254SDZ Evaluation Board Software Main Window

SOFTWARE OPERATION

The main window of the EVAL-AD5254SDZ software is divided into the following sections: QUICK COMMANDS, REGISTER ACCESS, WP, TOLERANCE, and MEMORY. The features of the main window are as follows:

- The QUICK COMMANDS section allows you to send the AD5254 quick commands directly to the AD5254.
- The REGISTER ACCESS section can be used to update the RDAC registers by typing a value into a window and clicking WRITE. Alternatively, you can send a customized I²C data word by manually switching the scroll bars from 0 to 1 or from 1 to 0, as desired, and then clicking SEND DATA. When WRITE is clicked or a quick command is executed, a write-read operation is performed, and the
- values displayed in this section are updated with the actual RDAC register values. This function can be used to verify whether the write operation was completed successfully. The scroll bars are updated upon each write transfer.
- The $\overline{\text{WP}}$ section enables or disables the AD5254 $\overline{\text{WP}}$ pin.
- The **TOLERANCE** section displays the stored tolerance of each internal resistor.
- The MEMORY section displays the data stored in the memory block. The data can be updated by switching the scroll bar from READ to WRITE, updating a particular window value, clicking UPDATE ALL or UPDATE SINGLE, and selecting the memory location to write.
- Clicking EXIT closes the program but does not reset the part.

EVALUATION BOARD SCHEMATICS AND ARTWORK

MULTICHANNEL

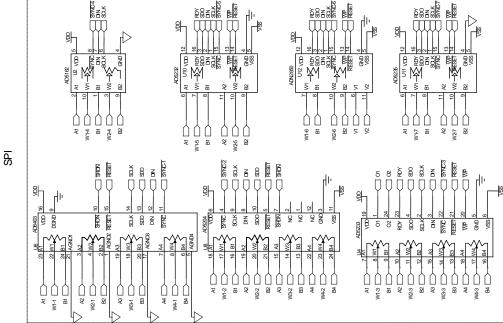


Figure 12. Schematic of Multiboard Digital Potentiometers

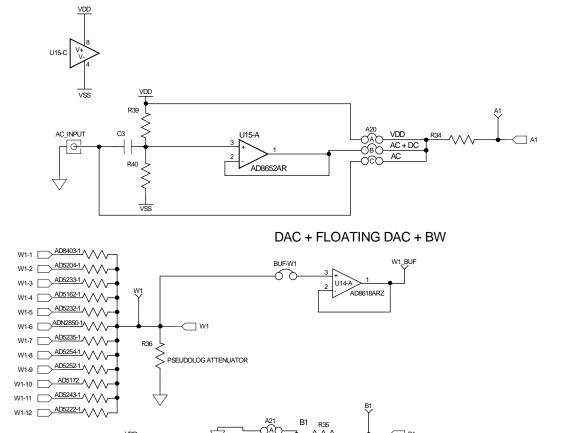


Figure 13. Schematic of Multiboard RDAC0 Circuits

U15-B

INVERTING AND NON-INVERTING WITH LINEAR AND PSEUDO-LOG GAIN

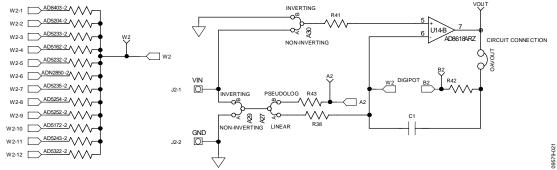
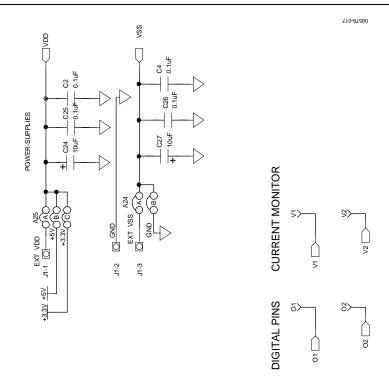


Figure 14. Schematic of Multiboard RDAC1 Circuits

POWER-SUPPLY



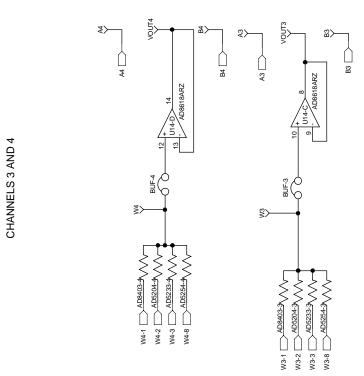


Figure 15. Schematic of AD5254 Power Supplies and Other Channels

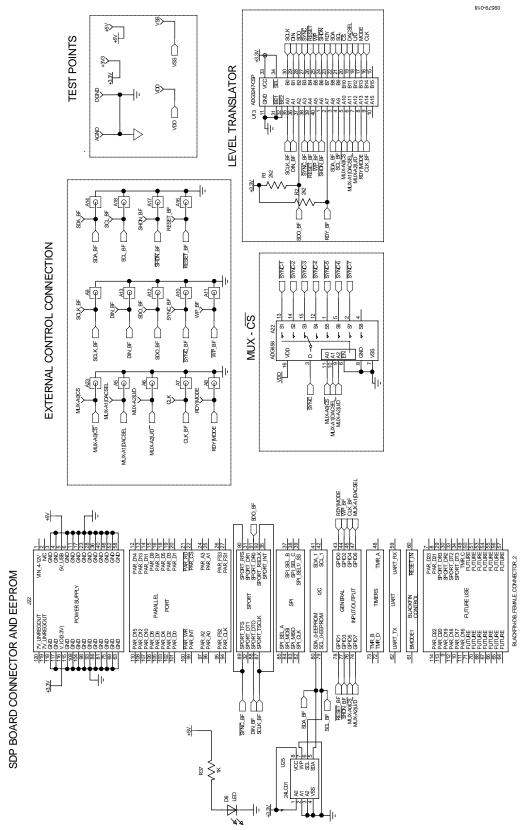


Figure 16. Schematic of SDP Connector

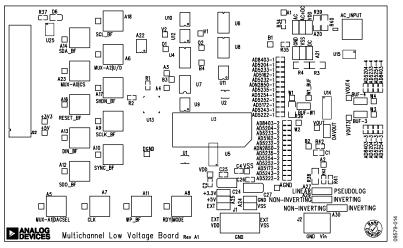


Figure 17. Component Side View

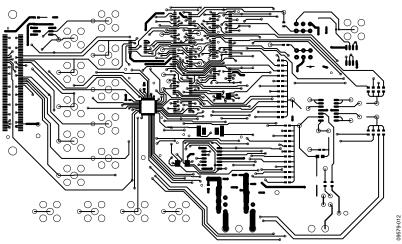


Figure 18. Component Placement Drawing

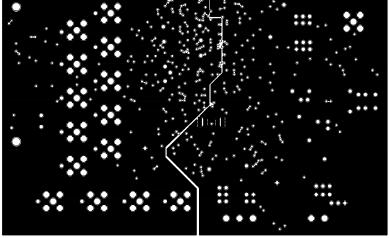


Figure 19. Layer 2 Side PCB Drawing

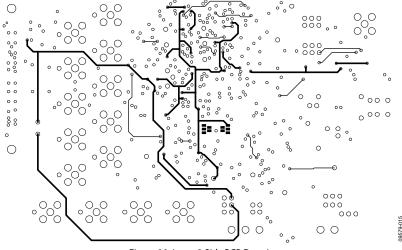


Figure 20. Layer 3 Side PCB Drawing

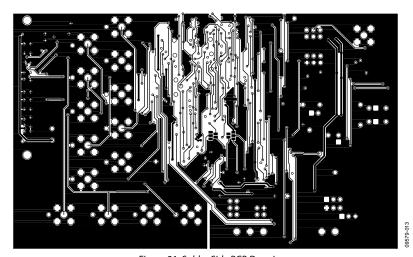


Figure 21. Solder Side PCB Drawing

ORDERING INFORMATION

BILL OF MATERIALS

Table 7.

Qty	Reference Designator	Description	Supplier ¹ /Part Number
1	C1	10 nF capacitor, 0805	FEC 1692285
4	C2, C4, C25, C26	0.1 μF capacitor, 0603	FEC 138-2224
1	C3	1 μF capacitor, 0402	FEC 1288253
2	C24, C27	10 μF capacitor, 1206	FEC 1611967
1	D6	LED, green	FEC 579-0852
1	J1	3-pin connector	FEC 151790
1	J2	2-pin connector	FEC 151789
1	J22	Receptacle, 0.6 mm, 120 way	Digi-Key H1219-ND
4	A20, A21, A24, A25	Header, 2-row, 36 + 36 way, and jumper socket, black	FEC 148-535 and FEC 150-410
3	A27, A29, A30	Header, 1-row, 3-way, and jumper socket, black	FEC 102-2248 and FEC 150-410
4	BUF-W1, OAVOUT, BUF-3, BUF-4	Header, 1-row, 2-way, and jumper socket, black	FEC 102-2247 and FEC 150-410
1	R41	1.78 kΩ resistor, 0603, 1%	FEC 1170811
2	R1, R2	2.2 kΩ resistor, 0603, 1%	FEC 933-0810
5		2.7 kΩ resistor, 1206, 1%	FEC 9337288
36	R3, R4, R38, R39, R40 AD5162-1, AD5162-2, AD5172-1,	0Ω resistor, 0603	FEC 9331662
	AD5172-2, AD5204-1, AD5204-2, AD5204-3, AD5204-4, AD5222-1, AD5222-2, AD5232-1, AD5232-2, AD5233-1, AD5233-2, AD5233-3, AD5233-4, AD5235-1, AD5235-2, AD5243-1, AD5243-2, AD5252-1, AD5252-2, AD5254-1, AD5254-2, AD5254-3, AD5254-4, AD8403-1, AD8403-2, AD8403-3, AD8403-4, ADN2850-1, ADN2850-2, R34, R35, R42, R43		
1	R37	1 kΩ resistor, 0603, 1%	FEC 933-0380
6	3.3 V, 5 V, DGND, AGND, VDD, VSS	Test point, PCB, black, PK100	FEC 873-1128
35	A1, A2, A3, A4, RDY MODE, RESET_BF, SCL_BF, SCLK_BF, SDA_BF, SDO_BF, SHDN_BF, SYNC_BF, MUX-A0 CS, MUX-A1 DACSEL, MUX-A2 U/D, O1, O2, DIN_BF, CLK, B1, B2, B3, B4, V1, V2, VOUT, VOUT2, VOUT3, VOUT4, W1, W1_BUF, W2, W3, W4, WP_BUF	Test point, PCB, red, PK100	FEC 873-1144
1	U1	AD5243	Analog Devices AD5243
1	U2	AD5162	Analog Devices AD5162
1	U3	AD5172	Analog Devices AD5172
1	U4	AD5233	Analog Devices AD5233
1	U5	AD5222	Analog Devices AD5222
1	U6	AD8403	Analog Devices AD8403
1	U7	AD5254	Analog Devices AD5254
1	U8	AD5204	Analog Devices AD5204
1	U9	AD5252	Analog Devices AD5252
1	U10	AD5232	Analog Devices AD5232
1	U11	AD5235	Analog Devices AD5235
1	U12	ADN2850	Analog Devices ADN2850
1	U13	ADG3247	Analog Devices ADG3247
1	U14	AD8618	Analog Devices AD8618
1	U15	AD8652	Analog Devices AD8652
1	A22	ADG658	Analog Devices ADG658
•		24LC64	FEC 975-8070

 $^{^{\}rm 1}$ FEC refers to Farnell Electronic Component Distributors; Digi-Key refers to Digi-Key Corporation.

NOTES

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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