MAC4DCM, MAC4DCN

Preferred Device

Triacs

Silicon Bidirectional Thyristors

Designed for high volume, low cost, industrial and consumer applications such as motor control; process control; temperature, light and speed control.

Features

- Small Size Surface Mount DPAK Package
- Passivated Die for Reliability and Uniformity
- Blocking Voltage to 800 V
- On−State Current Rating of 4.0 A RMS at 108°C
- High Immunity to dv/dt − 500 V/μs at 125°C
- High Immunity to di/dt − 6.0 A/ms at 125°C
- Epoxy Meets UL 94 V−0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V

    Machine Model, C > 400 V
- Pb−Free Packages are Available

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off−State Voltage (Note 1) (T_J = −40 to 125°C, Sine Wave, 50 to 60 Hz, Gate Open) MAC4DCM MAC4DCN	V_{DRM}, V_{RRM}	 600 800	V
On−State RMS Current (Full Cycle Sine Wave, 60 Hz, T_C = 108°C)	$I_{T(RMS)}$	4.0	A
Peak Non-Repetitive Surge Current (One Full Cycle Sine Wave, 60 Hz, T_J = 125°C)	I_{TSM}	40	A
Circuit Fusing Consideration (t = 8.3 msec)	I^2t	6.6	A^{2}sec
Peak Gate Power (Pulse Width ≤ 10 μsec, T_C = 108°C)	P_{GM}	2.0	W
Average Gate Power (t = 8.3 msec, T_C = 108°C)	$P_{G(AV)}$	1.0	W
Peak Gate Current (Pulse Width ≤ 20 μsec, T_C = 108°C)	I_{GM}	4.0	A
Peak Gate Voltage (Pulse Width ≤ 20 μsec, T_C = 108°C)	V_{GM}	5.0	V
Operating Junction Temperature Range	T_J	−40 to 125	°C
Storage Temperature Range	T_{stg}	−40 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
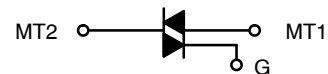
1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the device are exceeded.
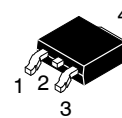
**TRIACS
4.0 AMPERES RMS
600 – 800 VOLTS**

MT2 —— MT1
G

MARKING DIAGRAMS

DPAK
CASE 369C
STYLE 6

YWW
AC
4DCxG
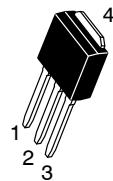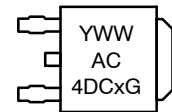
DPAK−3
CASE 369D
STYLE 6

YWW
AC
4DCxG
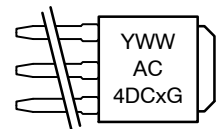
Y	= Year
WW	= Work Week
AC4DCx	= Device Code x= M or N
G	= Pb−Free Package

PIN ASSIGNMENT

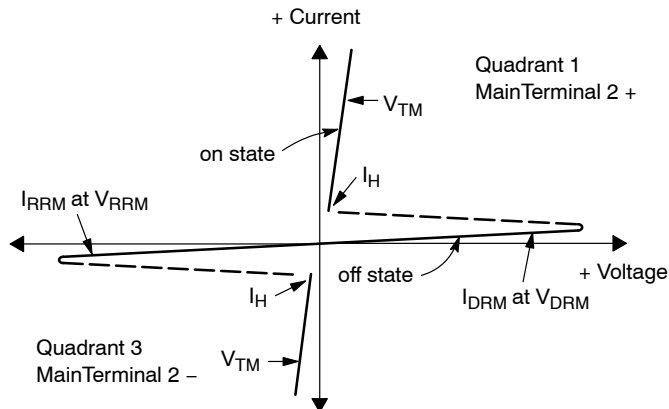|	
1	Main Terminal 1
2	Main Terminal 2
3	Gate
4	Main Terminal 2

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.
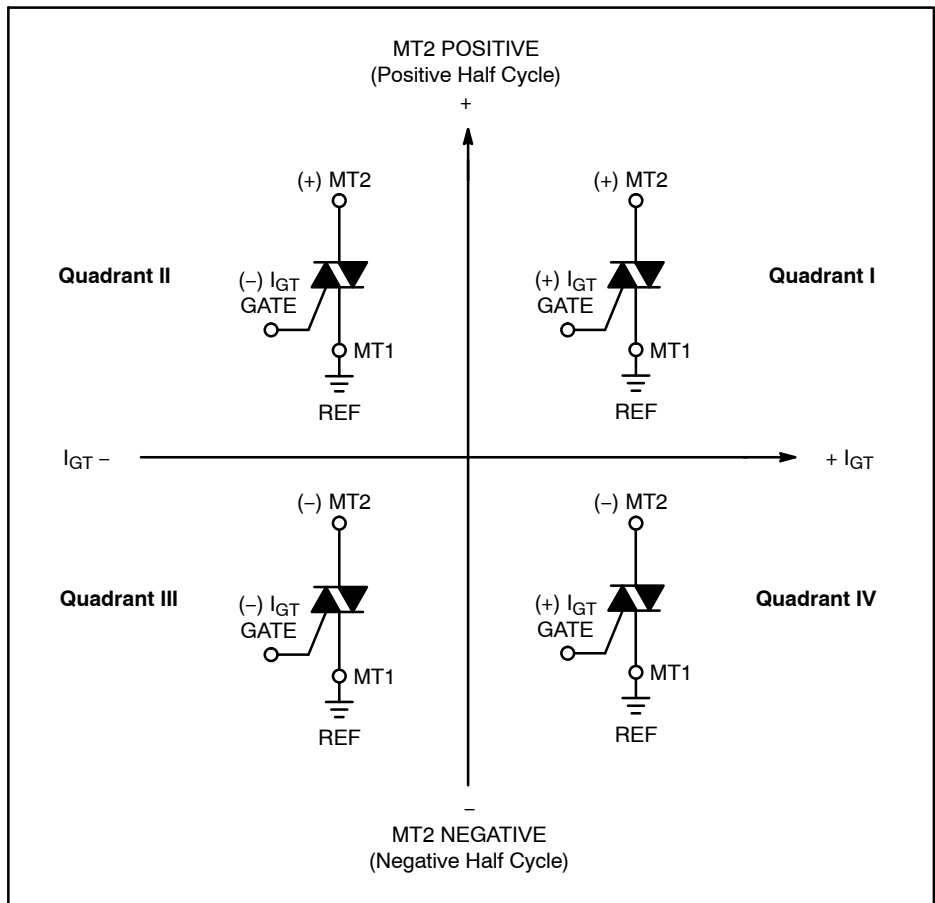
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, – Junction–to–Case – Junction–to–Ambient – Junction–to–Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.5 88 80	°C/W
Maximum Lead Temperature for Soldering Purposes (Note 3)	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted; Electricals apply in both directions)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Peak Repetitive Blocking Current (V_D = Rated V_{DRM}, V_{RRM}; Gate Open) T_J = 25°C T_J = 125°C	I_{DRM}, I_{RRM}	– –	– –	0.01 2.0	mA
ON CHARACTERISTICS					
Peak On–State Voltage (Note 4) (I_{TM} = ±6.0 A)	V_{TM}	–	1.3	1.6	V
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+) MT2(+), G(–) MT2(–), G(–)	I_{GT}	 8.0 8.0 8.0	 12 18 22	 35 35 35	mA
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+) MT2(+), G(–) MT2(–), G(–)	V_{GT}	 0.5 0.5 0.5	 0.8 0.8 0.8	 1.3 1.3 1.3	V
Gate Non–Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+); MT2(+), G(–); MT2(–), G(–) T_J = 125°C	V_{GD}	0.2	0.4	–	V
Holding Current (V_D = 12 V, Gate Open, Initiating Current = ±200 mA)	I_H	6.0	22	35	mA
Latching Current (V_D = 12 V, I_G = 35 mA) MT2(+), G(+) MT2(+), G(–) MT2(–), G(–)	I_L	 – – –	 30 50 20	 60 80 60	mA
DYNAMIC CHARACTERISTICS					
Rate of Change of Commutating Current (V_D = 400 V, I_{TM} = 4.0 A, Commutating dv/dt = 18 V/μsec, Gate Open, T_J = 125°C, f = 250 Hz, CL = 5.0 μF, LL = 20 mH, No Snubber) (See Figure 16)	di/dt(c)	6.0	8.4	–	A/ms
Critical Rate of Rise of Off–State Voltage (V_D = 0.67 X Rated V_{DRM}, Exponential Waveform, Gate Open, T_J = 125°C)	dv/dt	500	1700	–	V/μs

2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.
3. 1/8″ from case for 10 seconds.
4. Pulse Test: Pulse Width ≤ 2.0 msec, Duty Cycle ≤ 2%.

ORDERING INFORMATION

Device	Package Type	Package	Shipping
MAC4DCM–001	DPAK–3	369D	75 Units / Rail
MAC4DCM–1G	DPAK–3 (Pb–Free)	369D	75 Units / Rail
MAC4DCMT4	DPAK	369C	2500 / Tape & Reel
MAC4DCMT4G	DPAK (Pb–Free)	369C	2500 / Tape & Reel
MAC4DCN–001	DPAK–3	369D	75 Units / Rail
MAC4DCN–1G	DPAK–3 (Pb–Free)	369D	75 Units / Rail
MAC4DCNT4	DPAK	369C	2500 / Tape & Reel
MAC4DCNT4G	DPAK (Pb–Free)	369C	2500 / Tape & Reel

MAC4DCM, MAC4DCN

Voltage Current Characteristic of Triacs
(Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off−State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off−State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On−State Voltage
I_H	Holding Current

+ Current

Quadrant 1
MainTerminal 2 +

V_{TM}

on state

I_H

I_{RRM} at V_{RRM}

off state

+ Voltage

I_H

I_{DRM} at V_{DRM}

Quadrant 3
MainTerminal 2 −

V_{TM}

Quadrant Definitions for a Triac

MT2 POSITIVE
(Positive Half Cycle)

+

(+) MT2

Quadrant II

(−) I_{GT}
GATE

MT1

REF

(+) MT2

(+) I_{GT}
GATE

MT1

REF

Quadrant I

I_{GT} −

+ I_{GT}

(−) MT2

Quadrant III

(−) I_{GT}
GATE

MT1

REF

(−) MT2

(+) I_{GT}
GATE

MT1

REF

Quadrant IV

−
MT2 NEGATIVE
(Negative Half Cycle)

All polarities are referenced to MT1.
With in−phase signals (using standard AC lines) quadrants I and III are used.
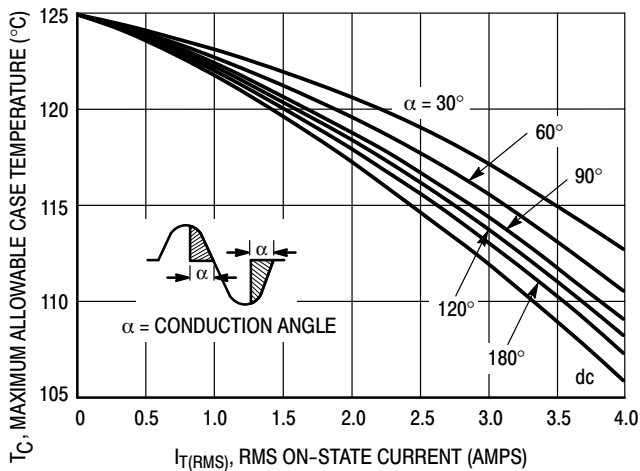
Figure 1. RMS Current Derating
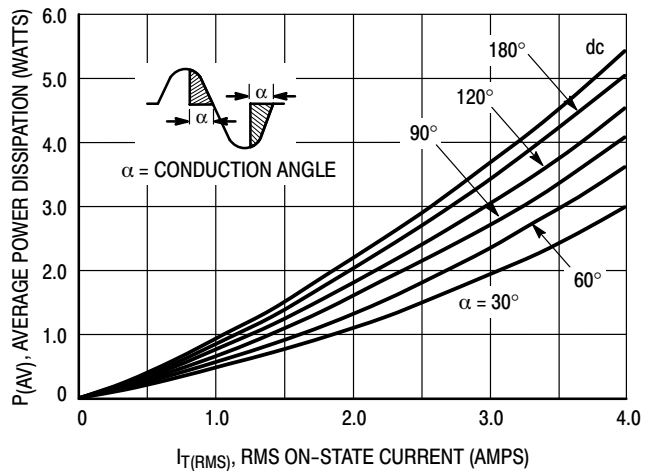
Figure 2. On−State Power Dissipation
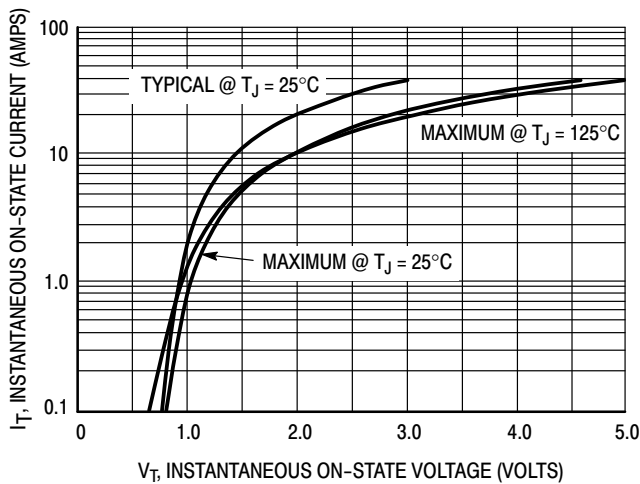
Figure 3. On−State Characteristics
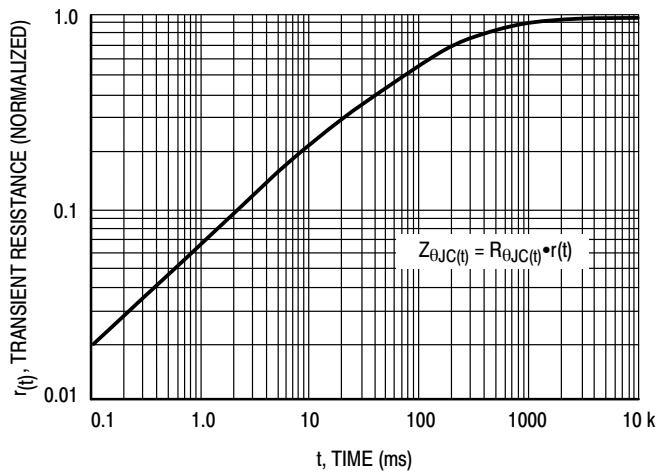
Figure 4. Transient Thermal Response
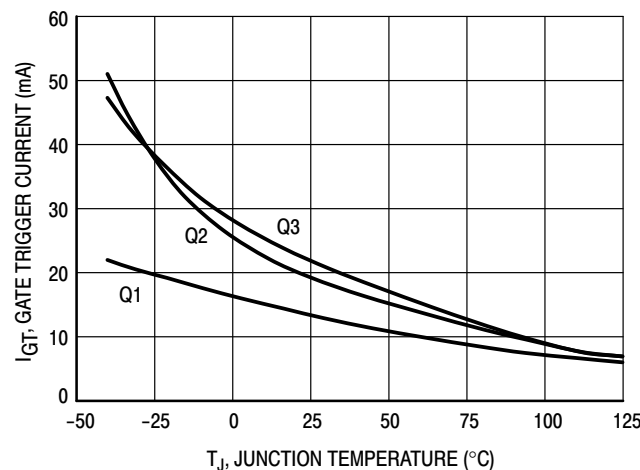
Figure 5. Typical Gate Trigger Current versus
Junction Temperature
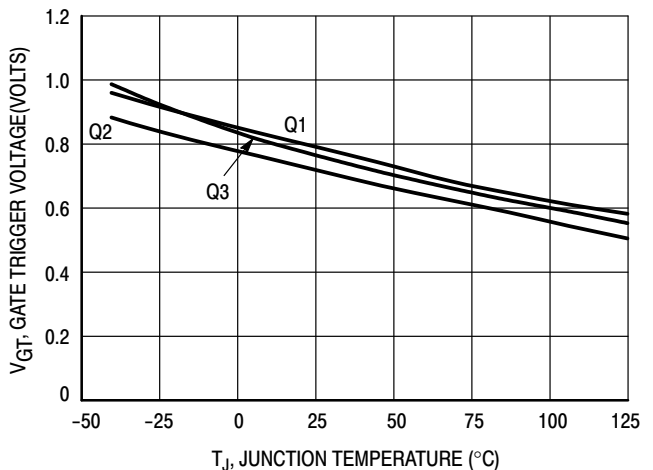
Figure 6. Typical Gate Trigger Voltage versus
Junction Temperature
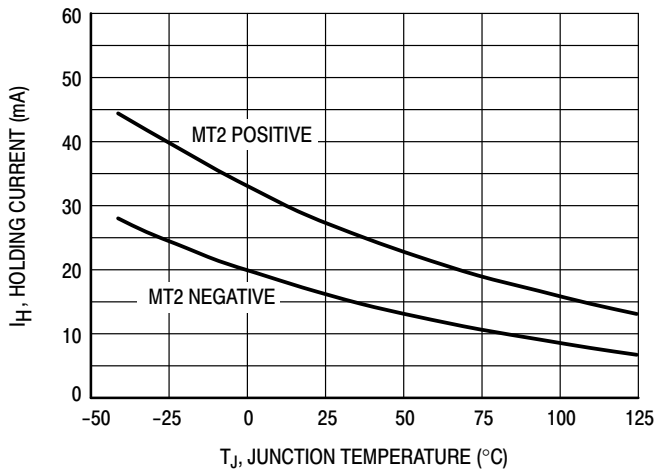
Figure 7. Typical Holding Current versus Junction Temperature
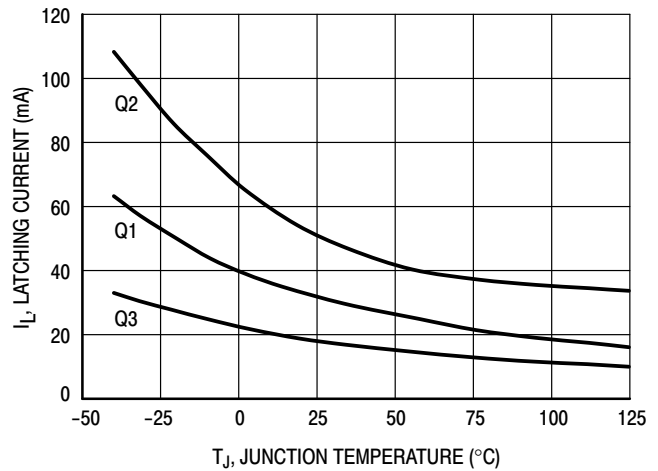
Figure 8. Typical Latching Current versus Junction Temperature
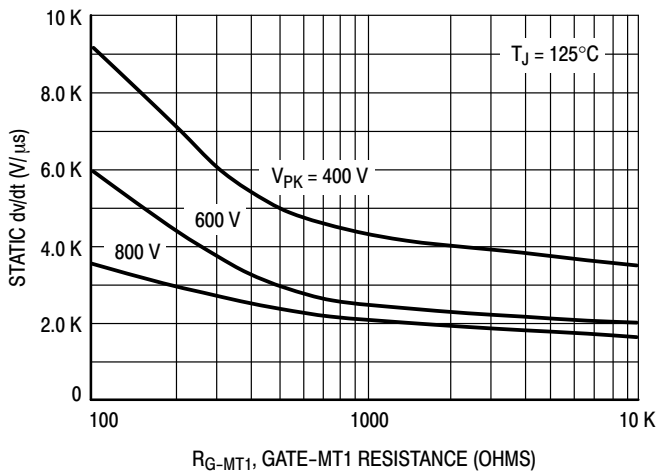
Figure 9. Exponential Static dv/dt versus Gate−MT1 Resistance, MT2(+)
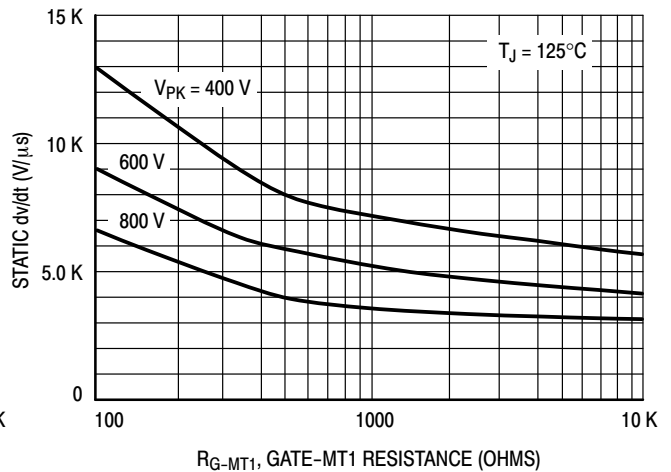
Figure 10. Exponential Static dv/dt versus Gate−MT1 Resistance, MT2(−)
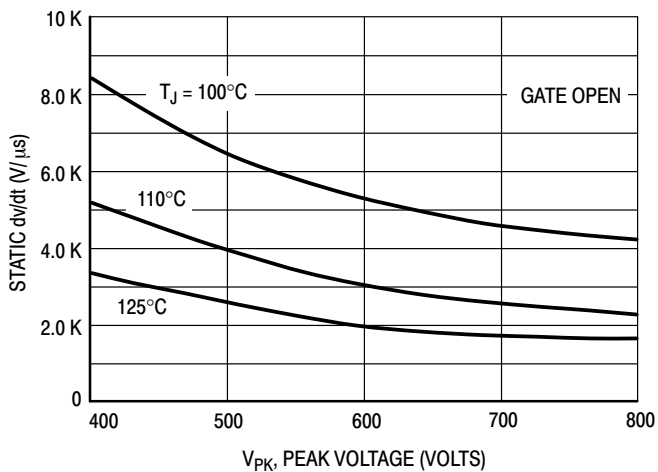
Figure 11. Exponential Static dv/dt versus Peak Voltage, MT2(+)
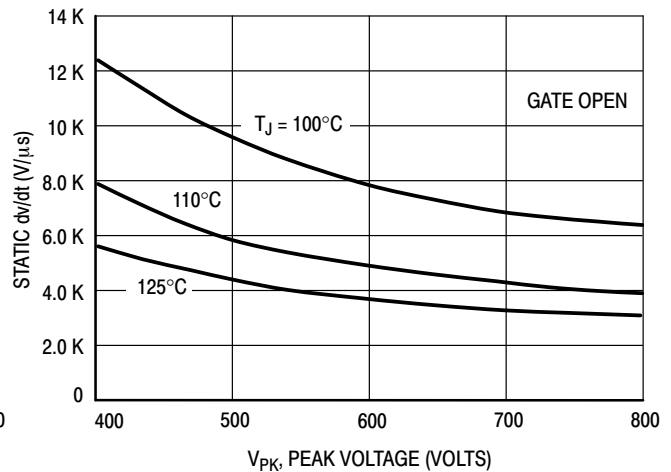
Figure 12. Exponential Static dv/dt versus Peak Voltage, MT2(−)

MAC4DCM, MAC4DCN
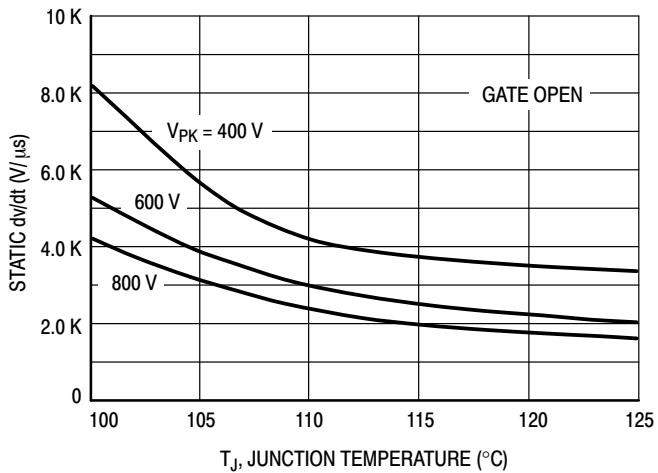
Figure 13. Typical Exponential Static dv/dt versus Junction Temperature, MT2(+)
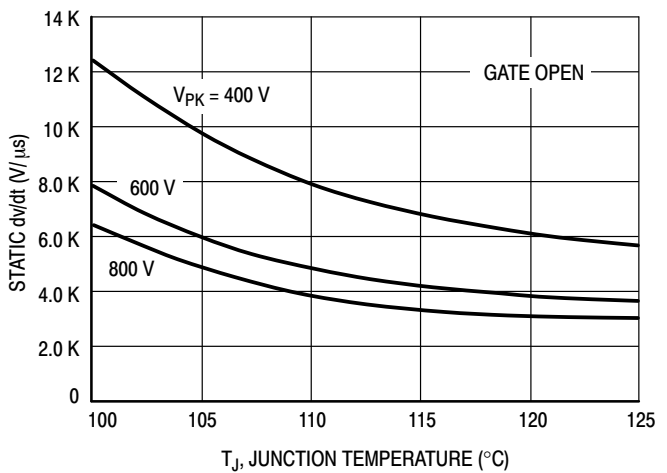
Figure 14. Typical Exponential Static dv/dt versus Junction Temperature, MT2(−)
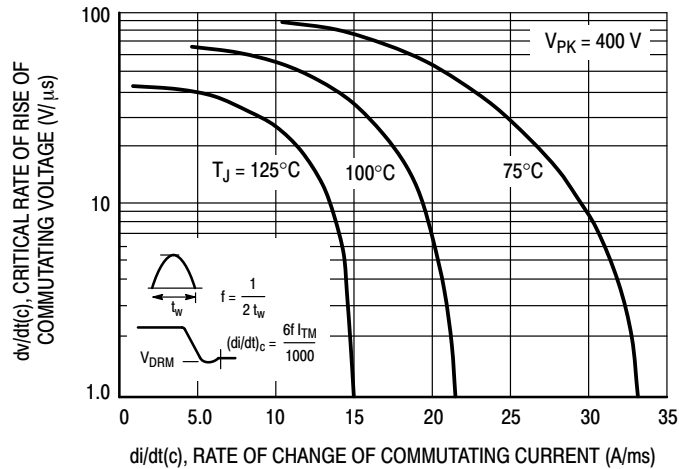
Figure 15. Critical Rate of Rise of Commutating Voltage

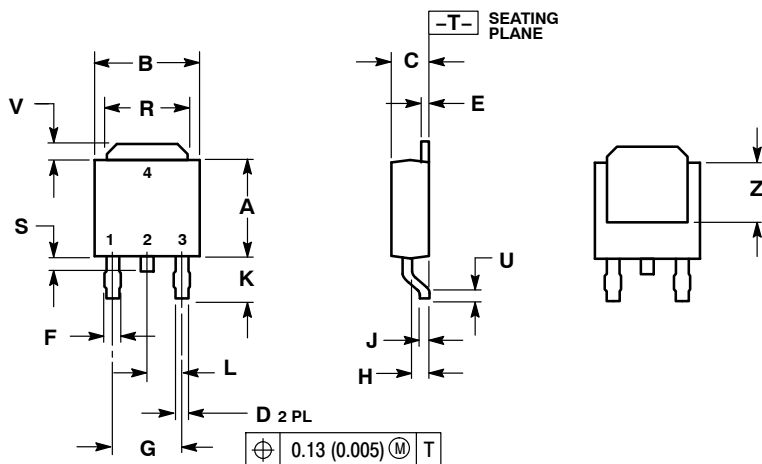$$f = \frac{1}{2\,t_w}$$

$$(di/dt)_c = \frac{6f\,I_{TM}}{1000}$$
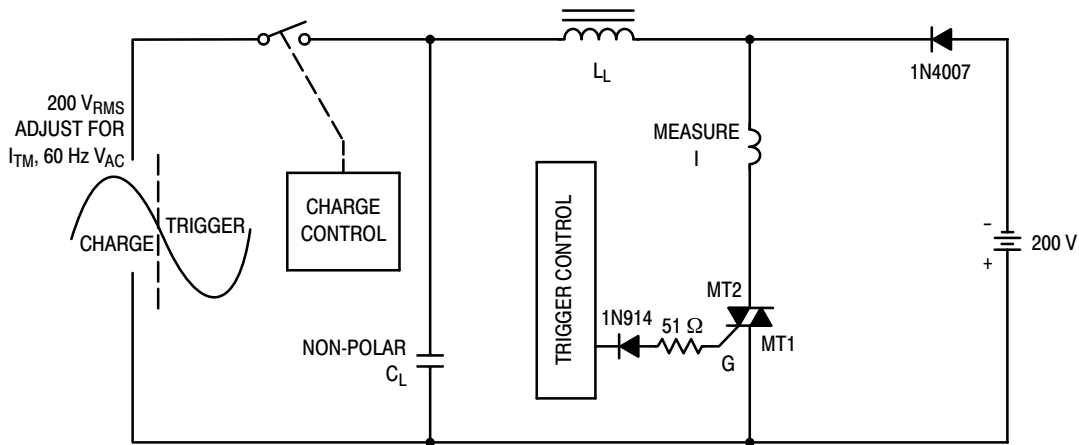
Note: Component values are for verification of rated $(di/dt)_c$. See AN1048 for additional information.

Figure 16. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Current $(di/dt)_c$
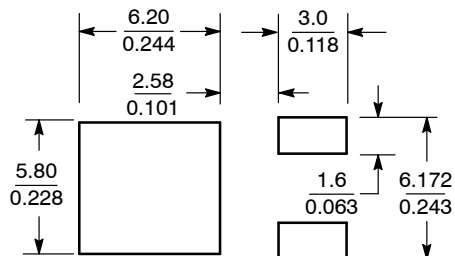
PACKAGE DIMENSIONS

DPAK
CASE 369C
ISSUE O

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

SOLDERING FOOTPRINT

SCALE 3:1 $\left(\dfrac{mm}{inches}\right)$

September 19, 2016 − Rev. 7

Publication Order Number:
MAC4DCM/D

PACKAGE DIMENSIONS

DPAK−3
CASE 369D−01
ISSUE B
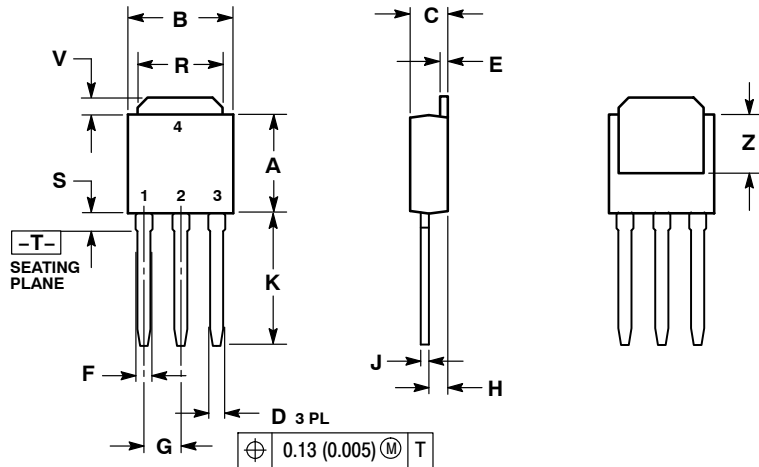
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E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	–––	3.93	–––

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

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