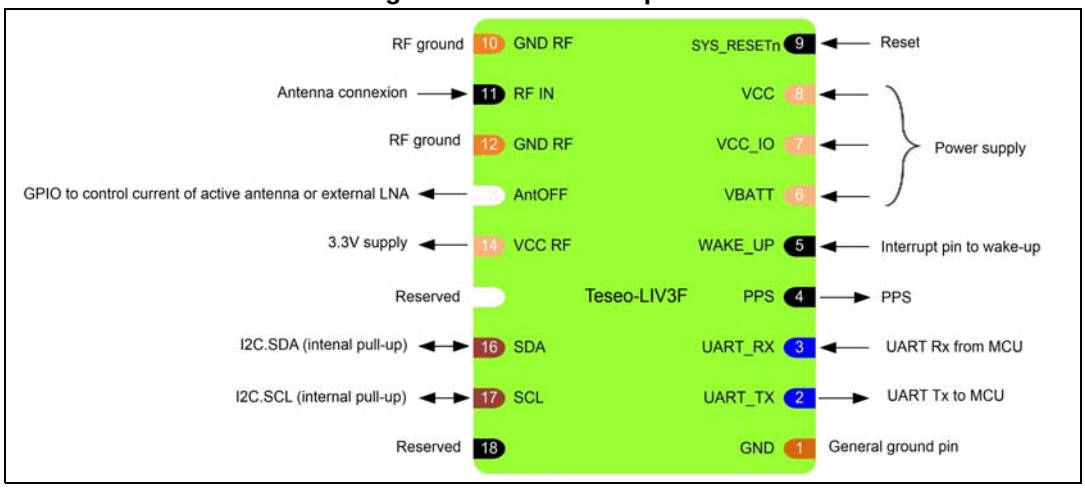
Introduction

Teseo-LIV3F is a tiny GNSS module sized 9.7 mm × 10.1 mm × 2.5 mm featuring STMicroelectronics® positioning receiver Teseo III. It is a standalone positioning receiver which embeds the new ST GNSS positioning engine capable of receiving signals from multiple satellite navigation systems, including GPS, Glonass or Beidou, Galileo and QZSS.

It embeds a 16M-Bit serial Flash.

In *Figure 1* pinout of the module is represented as follows:

Figure 1. Teseo-LIV3F pinout



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1 Power

Teseo-LIV3F is supplied by 3 power pins: VCC (pin8), VCC_IO (pin7) and VBAT (pin6).

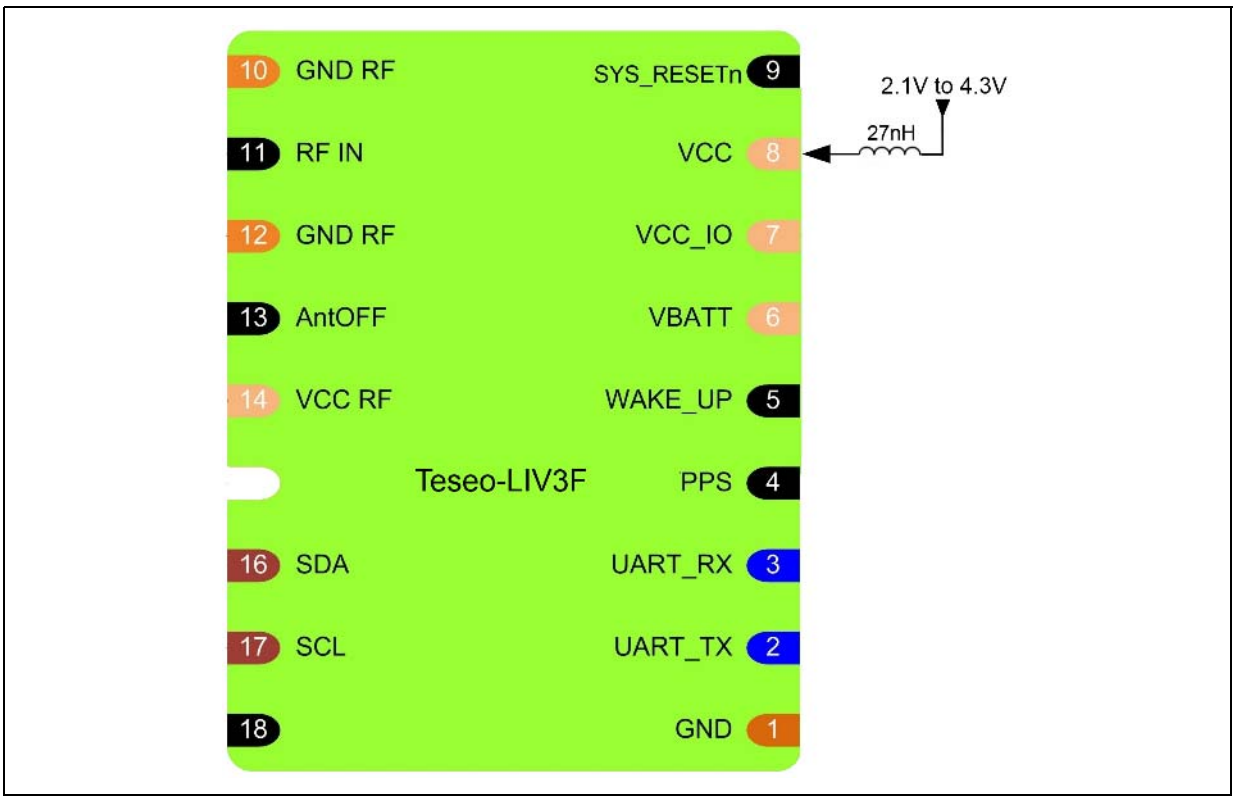
1.1 VCC (pin8)

VCC is the main supply. V_{CC} limiting values are: 2.1 V - 4.3 V.

At startup or during low power application current can change suddenly. It is important that supply IC is able to provide this current variation.

Take care that interference on VCC power line could degrade Teseo-LIV3F sensitivity performance, to avoid that it's recommended a 27 nH inductor (Murata LQG15HS27NJ02) as shown in *Figure 2: Inductor on VCC power line*.

Figure 2. Inductor on VCC power line



The suggested inductor on the VCC power line is able to recover interference coming from VCC power line.

1.2 VBAT (pin6)

VBAT is the supply for the low power domain backup: backup RAM and RTC.

VBAT can be either connected to VCC or it can be supplied by a dedicated supply always ON. When VBAT supply is kept ON during low power mode to allow fast recovery of GNSS fix

VBAT prevents current flow as soon as VBAT is lower than VCC. It is important when VBAT is supplied with small battery and especially if battery is not rechargeable.

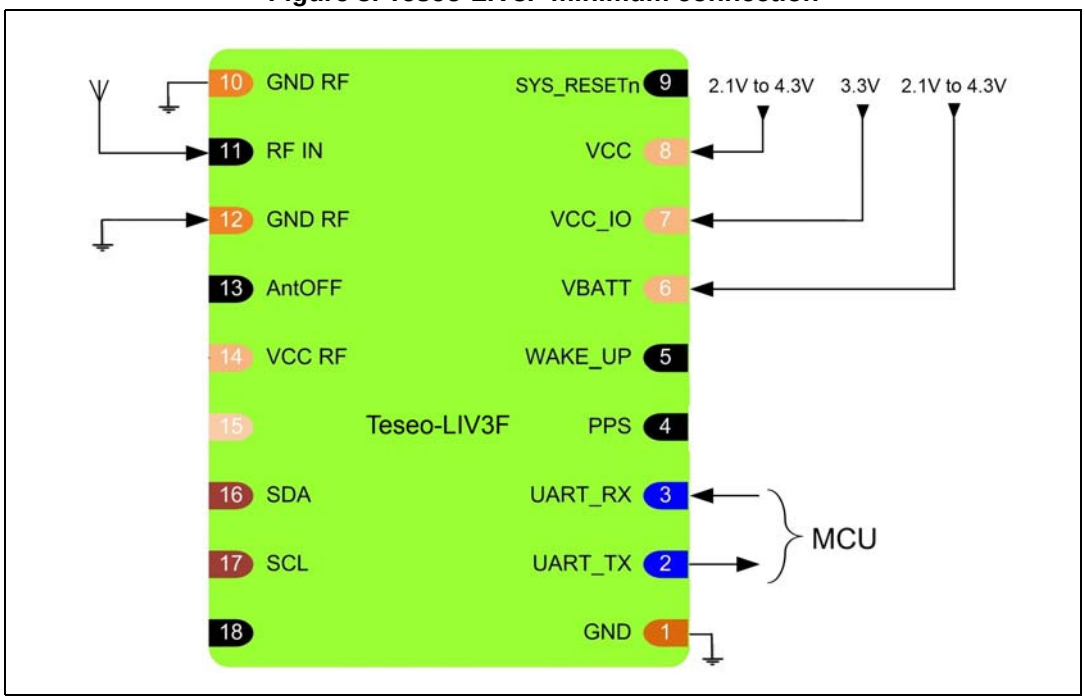
VBAT range can be from 2.1 V to 4.3 V.

1.3 VCC_IO (pin7)

VCC_IO is 3.3 V.

Figure 3 shows the minimum connection to make Teseo-LIV3F GNSS working.

Figure 3. Teseo-LIV3F minimum connection



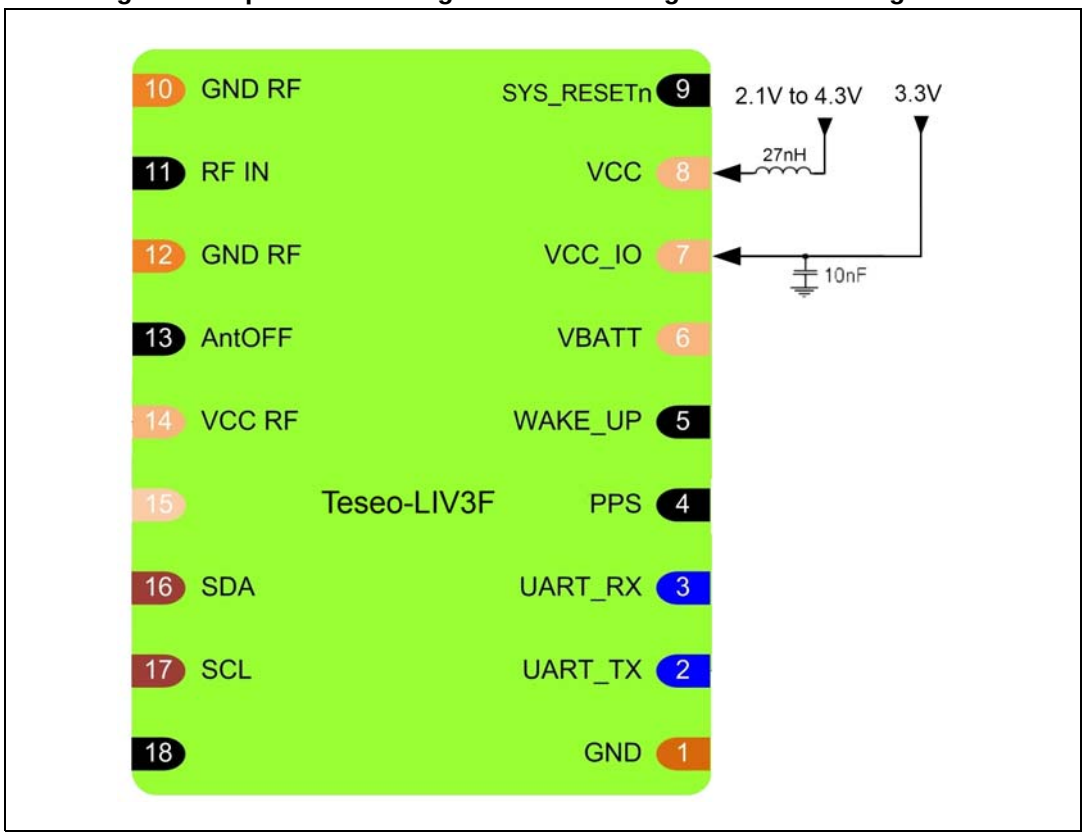
1.4 VCC_RF (pin14)

VCC_RF is an output image of VCC with a filtering for LNA or active antenna supply.

1.5 Power supply design reference

To reduce and filter the noise coming from the external regulator it's suggested a 10nF capacitor between VCC_IO and ground as shown in *Figure 4*.

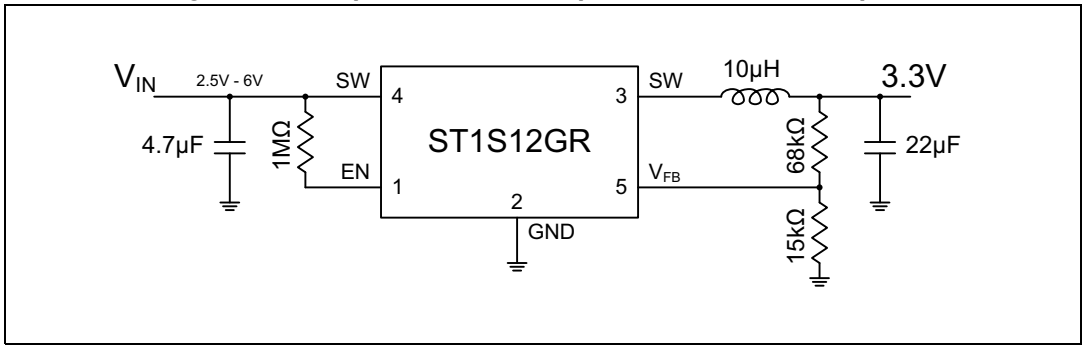
Figure 4. Capacitors filtering the noise coming from external regulators



1.6 Current consumption optimization

Use of an SMPS at 2.1V to supply VCC is recommended to optimize current consumption. Here is an application example with ST1S12GR with an efficiency around 85%.

Figure 5. Example of SMPS to improve current consumption



If VCC_IO is also supplied by an SMPS, this will reach the lowest current consumption.

2 Reserved (pin15, 18)

In Teseo-LIV3F pin15 and 18 are reserved.

3 Interfaces

3.1 I2C (pin16, 17)

Teseo-LIV3F supports I2C slave mode only.

Internal 10 KΩ pull-up resistor on VCC_IO is present. It is important to avoid having other pull-up for current leakage in low power mode.

3.2 UART (pin2, 3)

UART is a Universal Asynchronous Receiver/Transmitter that supports much of the functionality of the industry-standard 16C650 UART.

These UARTs vary from industry-standard 16C650 on some minor points which are:

- Receive FIFO trigger levels
- The deltas of the modem status signals are not available
- 1.5 stop bit is not supported
- Independent receive clock feature is not supported

4 I/O pins

4.1 PPS (pin4)

PPS is the time pulse every one second. It can be configured with different condition of pulses.

4.2 Wake_Up (pin5)

It is an external interrupt that is used to wake-up Teseo-LIV3F for asynchronous wake-up during standby software for instance.

It can be activated by a GPIO from host for instance. Wake_Up signal is active high.

4.3 SYS_RESETn (pin9)

It can force a Teseo-LIV3F under reset.

Reset signal is active low.

Host processor must have full control of this pin to guarantee the Teseo-LIV3F's firmware upgrade support.

4.4 RF_IN (pin10)

It is the RF input.

4.5 AntOFF (pin13)

AntOFF is a GPIO used to switch OFF external LNA or switch OFF current for the active antenna.

A 10 kΩ pull down is necessary to ensure a low level during standby period.

5 Standby modes

Standby mode, is the mode where only low power backup domain is running. It means VBAT must always be maintained. It allows to have very low current consumption and fast GNSS reacquisition at the end of the standby time due to RTC.

Teseo-LIV3F offers 2 different ways of standby:

- Hardware standby
- Software standby

As IO buffers are not supplied during standby mode, it is important to keep all IO without external voltage to avoid any current leakage. UART_RX is an exception it can be left high.

5.1 Software standby

Software standby is activated by the binary for periodic standby. More details of how to set it are in the Software Manual. As HW standby, all supplies are kept ON.

Periodic fixes are from 5 s up to 24hours between 2 fixes.

It ensures a current below 20 µA on Teseo-LIV3F. Be careful that VCC_RF is ON during this standby, then in case of active antenna or external LNA, it is important to switch them OFF.

5.2 Hardware standby

This standby is ensured by switching OFF VCC (pin 6) and VCC_IO (pin 7) supplies and setting SYS_RESETn (pin 9) to 0 V. It can be activated asynchronously from GNSS binary with one GPIO switching OFF the supplies from a host.

During this standby only VBAT (pin 6) is kept ON.

It ensures a current below 15 µA. During this standby mode VCC_RF (pin 14) is OFF.

6 Front ends management

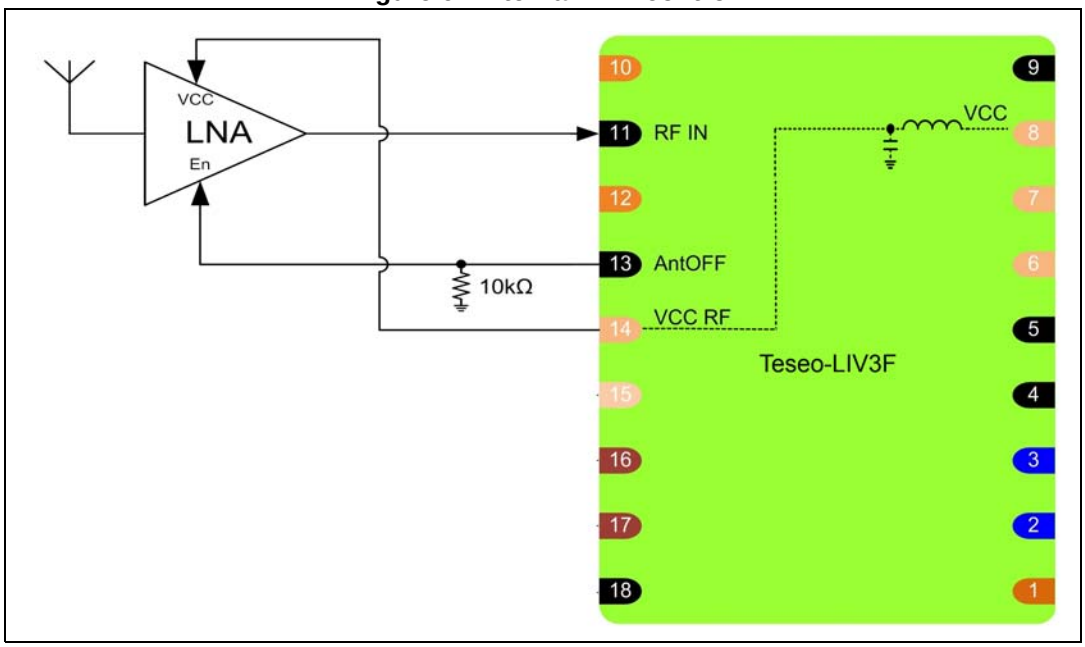
RF input impedance is 50 Ω.

6.1 External LNA

External LNA means a passive antenna used with an LNA on the same PCB as Teseo-LIV3F module. To optimize power consumption during low power mode if needed, the LNA should have an enable pin compatible with VCC_IO to be switched OFF/ON.

Here is a block diagram describing the connection.

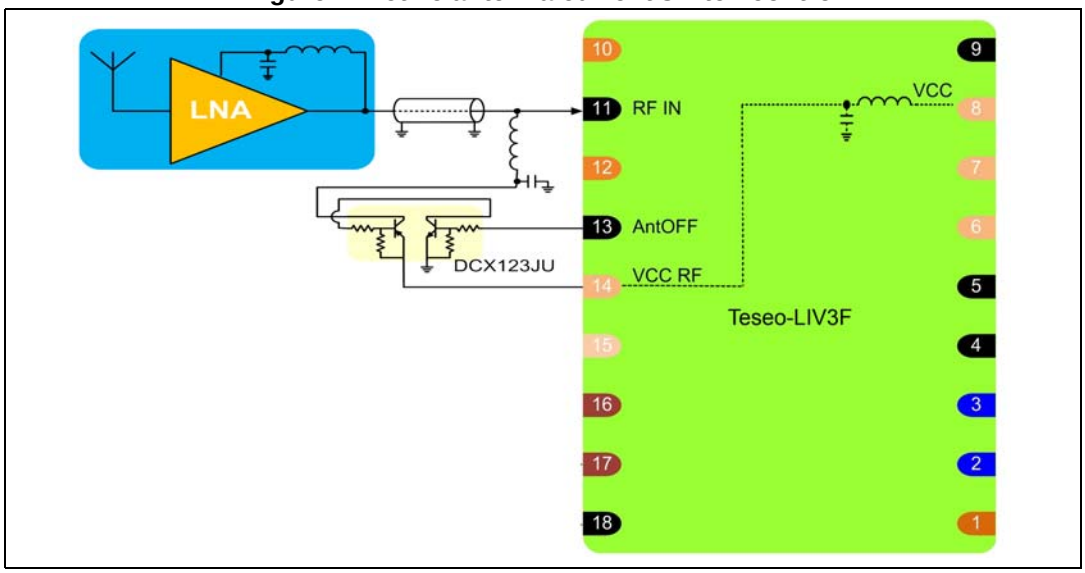
Figure 6. External LNA control



6.2 Active antenna

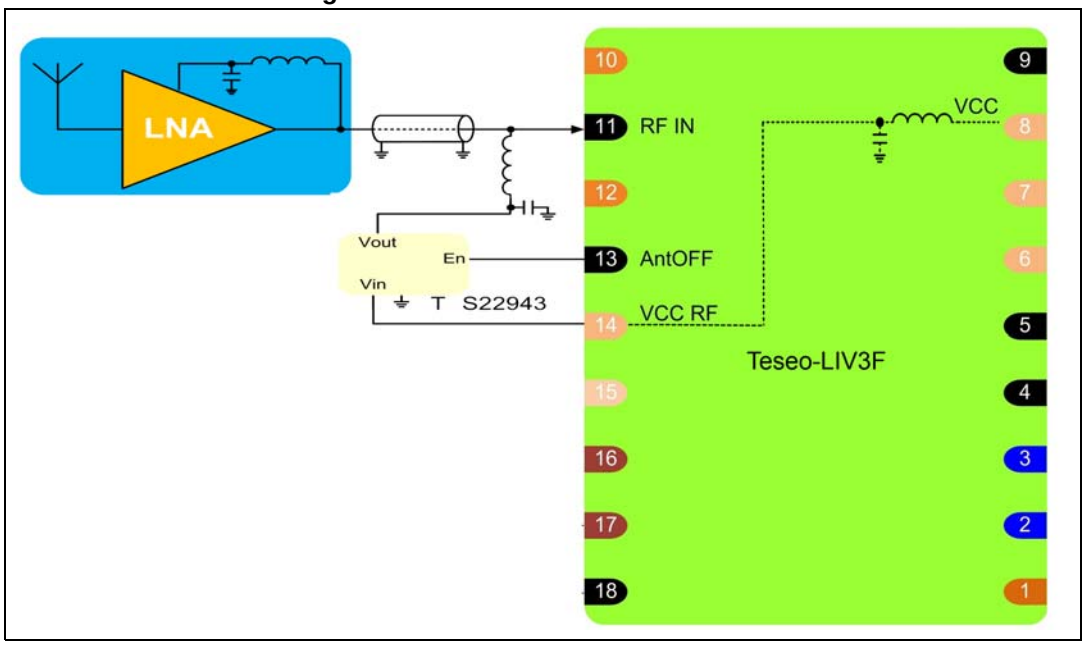
For RF passive components, ST recommends the usage of 0402 (1Ãx0.5mm) components. Please choose the RF ground layer to be able to get 50ohms RF line width as close as possible to components pads.

Figure 7. Active antenna current switch control



To improve the functionality, a current limiter could be used in order to prevent any short circuit on the antenna see *Figure 8*.

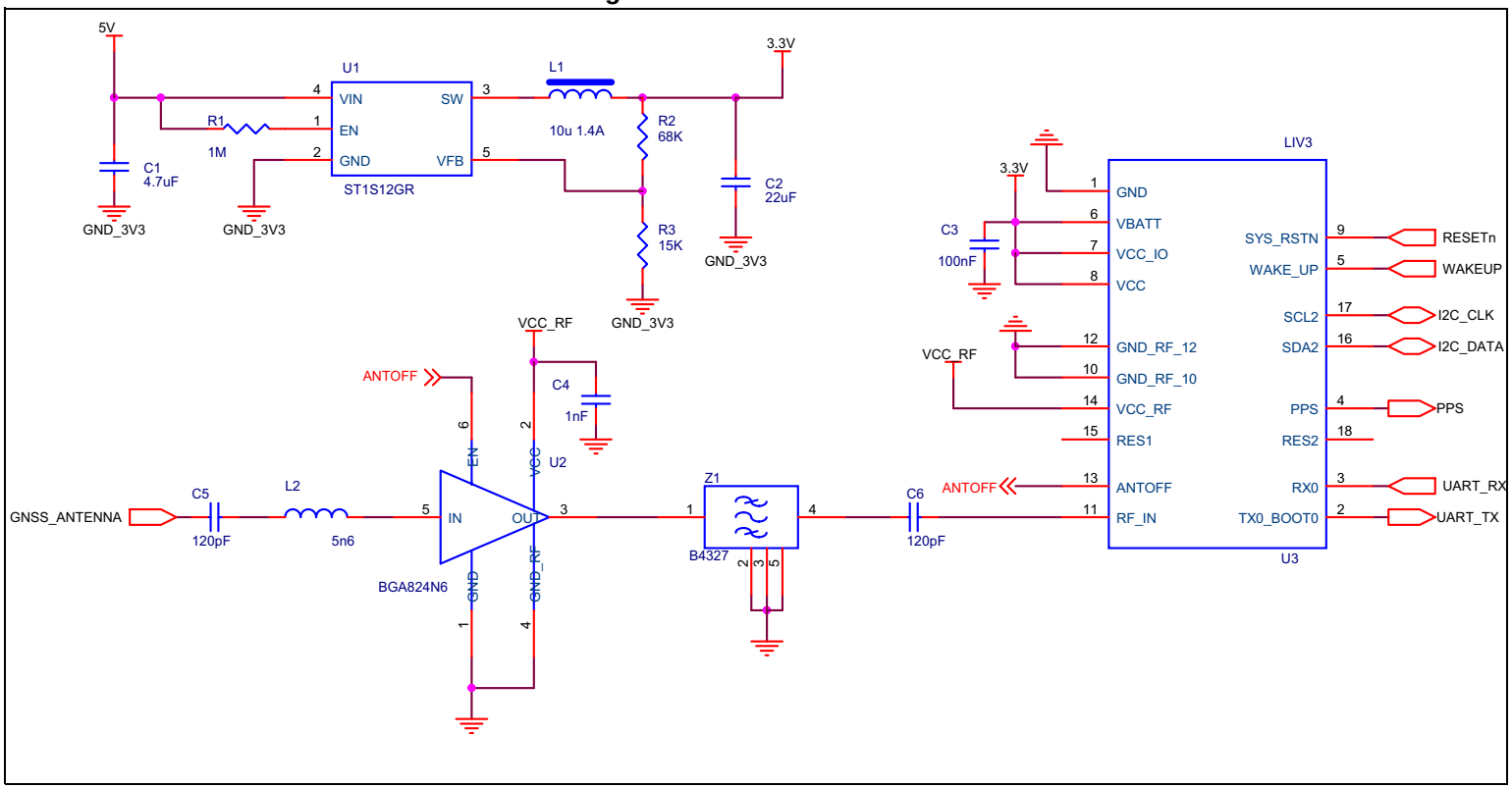
Figure 8. Active antenna current sense



7 Reference schematic and BOM

7.1 Schematic

Figure 9. General schematic



7.1.1 Bill of material

Table 1. Bill of material

Refs	Value	Description	Manufacturing 1		Manufacturing 2	
			Name	Part number	Name	Part number
C1	4u7	Surface mount 0603 capacitor ceramic 4.7 µF, 10% 10V X7S 4µ7; 10; X7S	Murata	GRM188C71A475 KE11		
C2	22 uF	Capacitor, Ceramic, SMD, MLCC, Temperature Stable, Class II, 22 µF, +/-20%, 6.3 V, X5R, 0805	KEMET	C0805C226M9PAC TU		
C3	100 n	Surface mount, general purpose multilayer ceramic chip capacitor 100n; 50V; X7R; +/-10%	TDK	C1608X7R1H104K T	Murata	GRM188R71H104K A93
C4	1 nF	Automotive Grade Surface mount 0402 capacitor ceramic 1 nF, 10% 50 V X7R 1 nF; 50; X7R	Murata	GCM155R71H102 KA37	TDK	CGA2B2X7R1H102 K050BA
C5,C 6	120 pF	Automotive Grade Surface mount 0402 capacitor ceramic 120 pF, 5% 50 V C0G 120 pF; 50; C0G	Murata	GCM1555C1H121 JA16	TDK	CGA2B2C0G1H121 J050BA
L1	10 µ	Surface mount magnetically shielded, wire wound inductor for power line applications. 10 µ; 1.4 A	TDK	LTF5022T-100M1R4-LC		
L2	5n6H	Surface mount wire wound inductor. 5n6H; 3%; 0.76 A	Coilcraft	0402CS-5N6XJLU	Murata	LQW15AN5N6G80 D+00-21
R1	1 M	Surface mount chip resistor 1 M; 5%; 0.1 W	Rohm	MCR03EZPJ105		
R2	68 K	Surface mount chip resistor 68 K; 1%; 0.1 W	Rohm	MCR03EZPF683		
R3	15 K	Surface mount chip resistor 15 K; 1%; 0.1 W	Rohm	MCR03EZPF153	Yageo	AC0603FR-0715KL
U1	ST1S12GR	Synchronous rectification adjustable step-down switching regulator ST1S12GR; 0.7; 1.7	STMicroelectronics	ST1S12GR TSOT23-5L		
U2	BGA824N6	Low Noise Amplifier for GPS, GLONASS, Galileo and Compass BGA824N6	Infineon	BGA824N6		
Z1	B4327	Automotive SAW RF filter for GPS+COMPASS+GLONASS	Epcos	B39162B4327P810		
U3	LIV	TESEOIII module SMPS version	STMicroelectronics	LIV3F		

8 Layout recommendation

To guarantee good RF performance, 0402 components are preferable because they avoid having too big component pads compared with RF 50 ohms line.

Place parallel components pads on 50 ohms line as in *Figure 10*.

Figure 10. Placing parallel component pads on 50 ohms line

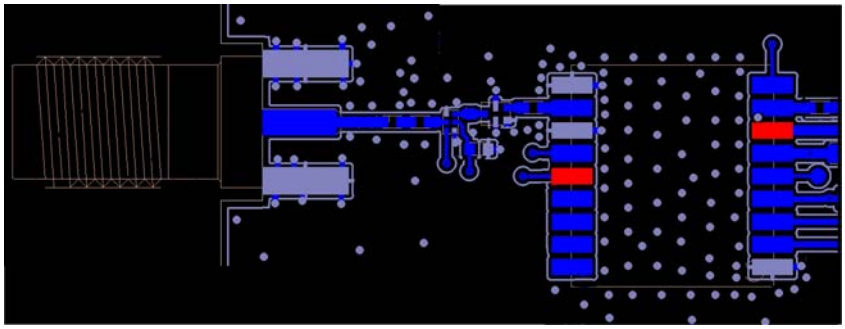
For 50 ohms line bypassing it's suggested to superimpose the pad of one component on the pad of the other one as in *Figure 11*.

Figure 11. Reuse pads of one component on the line bypassing

Place ground vias below Teseo-LIV3F all around and in the middle and also around the 3 ground pins.

The following layout presents layout recommendation to ensure the best performances of Teseo-LIV3F. ST heartily recommends having a maximum of ground vias below the module as illustrated in the above figure. In case of difficulties for all these vias, ensure to have several vias at least around the 3 ground pins (pin1, pin10 and pin 12).

Figure 12. Layout proposal



It is important to have 50 ohms RF traces width as close as possible to components pads size to avoid too much impedance jumps.

When possible, avoid any trace below Teseo-LIV3F module.

9 Revision history

Table 2. Document revision history

Date	Revision	Changes
08-Sep-2017	1	Initial release.
09-May-2018	2	Added *Chapter 8: Layout recommendation*.
02-Jul-2018	3	Updated *Chapter 8: Layout recommendation*. Updated *Figure 10: Placing parallel component pads on 50 ohms line*, *Figure 11: Reuse pads of one component on the line bypassing* and *Figure 12: Layout proposal*. Minor text changes.