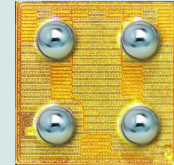


EPC2037 – Enhancement Mode Power Transistor

 $V_{DSS}, 100\text{ V}$
 $R_{DS(on)}, 550\text{ m}\Omega$
 $I_D, 1.7\text{ A}$


Gallium Nitride is grown on Silicon Wafers and processed using standard CMOS equipment leveraging the infrastructure that has been developed over the last 60 years. GaN's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.



EPC2037 eGaN® FETs are supplied only in passivated die form with solder bumps.
Die size: 0.9 mm x 0.9 mm

Applications

- High Speed DC-DC Conversion
- Wireless Power Transfer
- LiDAR/Pulsed Power Applications
- Class-D Audio

Benefits

- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra Low Q_G
- Ultra Small Footprint

www.epc-co.com/epc/Products/eGaNfETs/EPC2037.aspx

Maximum Ratings

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5ms pulses at 150°C)	120	
I_D	Continuous ($T_A = 25^\circ\text{C}$, $R_{\theta JA} = 44^\circ\text{C/W}$)	1.7	A
	Pulsed (25°C , $T_{PULSE} = 300\ \mu\text{s}$)	2.4	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}$, $I_D = 125\ \mu\text{A}$	100			V
I_{DSS}	Drain Source Leakage	$V_{DS} = 80\text{ V}$, $V_{GS} = 0\text{ V}$		10	100	μA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$		0.1	1	mA
	Gate-to-Source Reverse Leakage	$V_{GS} = -4\text{ V}$		10	100	μA
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 0.8\text{ mA}$	0.8	1.5	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}$, $I_D = 0.1\text{ A}$		400	550	$\text{m}\Omega$
V_{SD}	Source-Drain Forward Voltage	$I_S = 0.3\text{ A}$, $V_{GS} = 0\text{ V}$		2.5		V

All measurements were done with substrate shorted to source.

Thermal Characteristics

		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	14	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	79	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	100	°C/W

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Dynamic Characteristics (T _J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C _{ISS}	Input Capacitance	V _{DS} = 50 V, V _{GS} = 0 V		14	17	pF
C _{RSS}	Reverse Transfer Capacitance			0.1		
C _{OSS}	Output Capacitance			6.5	10	
C _{OSS(ER)}	Effective Output Capacitance, Energy Related (Note 2)	V _{DS} = 0 to 50 V, V _{GS} = 0 V		9.5		
C _{OSS(TR)}	Effective Output Capacitance, Time Related (Note 3)			12		
R _G	Gate Resistance			0.5		Ω
Q _G	Total Gate Charge	V _{DS} = 50 V, V _{GS} = 5 V, I _D = 0.1 A		115	145	pC
Q _{GS}	Gate to Source Charge	V _{DS} = 50 V, I _D = 0.1 A		32		
Q _{GD}	Gate to Drain Charge			25		
Q _{G(TH)}	Gate Charge at Threshold			24		
Q _{OSS}	Output Charge	V _{DS} = 50 V, V _{GS} = 0 V		600	900	
Q _{RR}	Source-Drain Recovery Charge			0		

Note 2: C_{OSS(ER)} is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
 Note 3: C_{OSS(TR)} is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

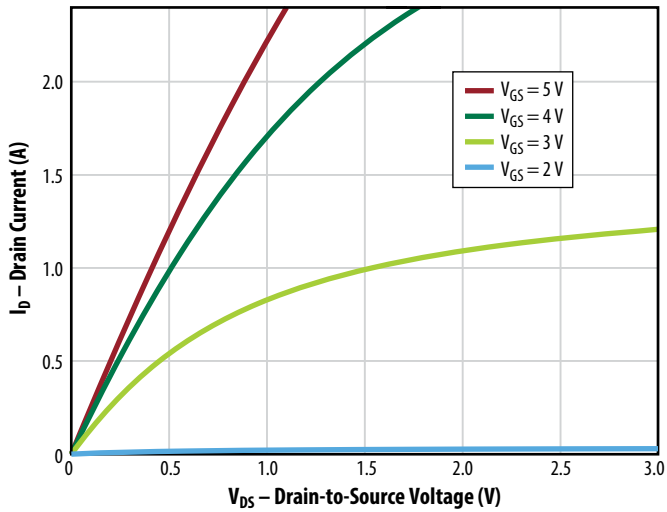


Figure 2: Transfer Characteristics

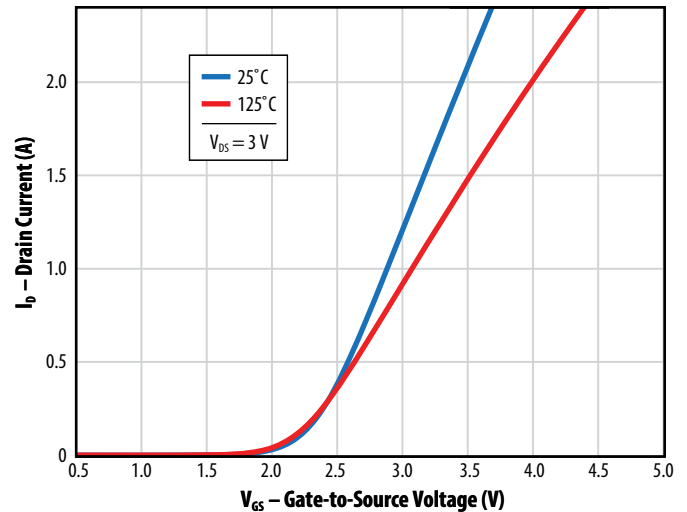


Figure 3: R_{DS(on)} vs. V_{GS} for Various Drain Currents

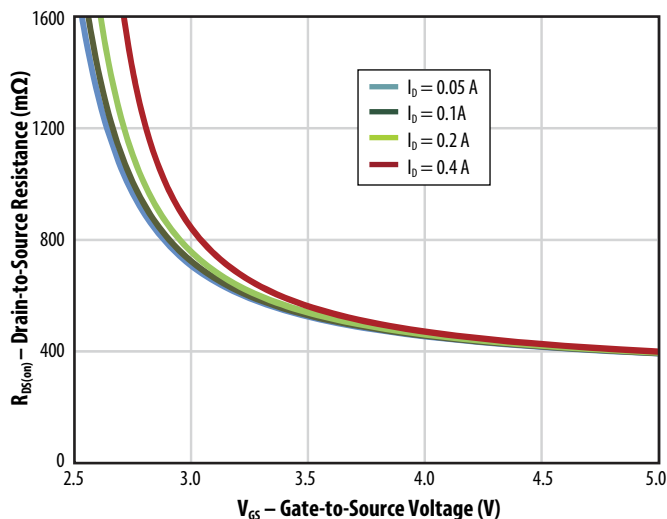


Figure 4: R_{DS(on)} vs. V_{GS} for Various Temperatures

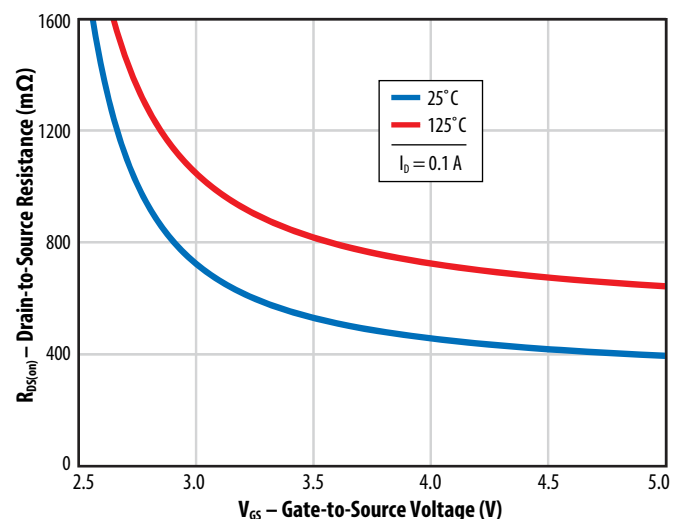


Figure 5a: Capacitance (Linear Scale)

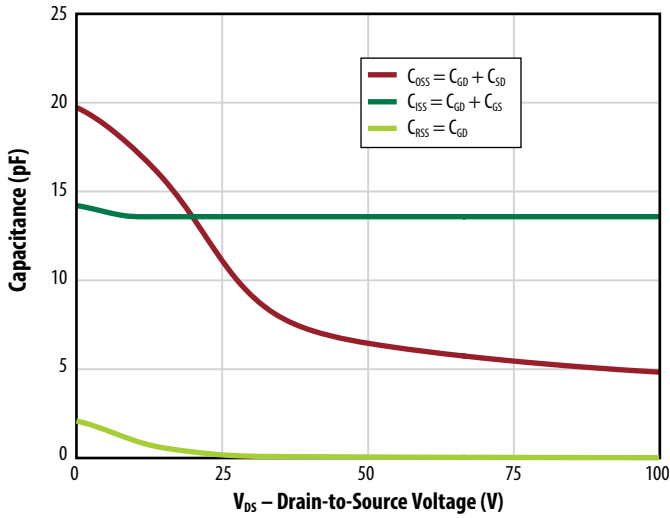


Figure 5b: Capacitance (Log Scale)

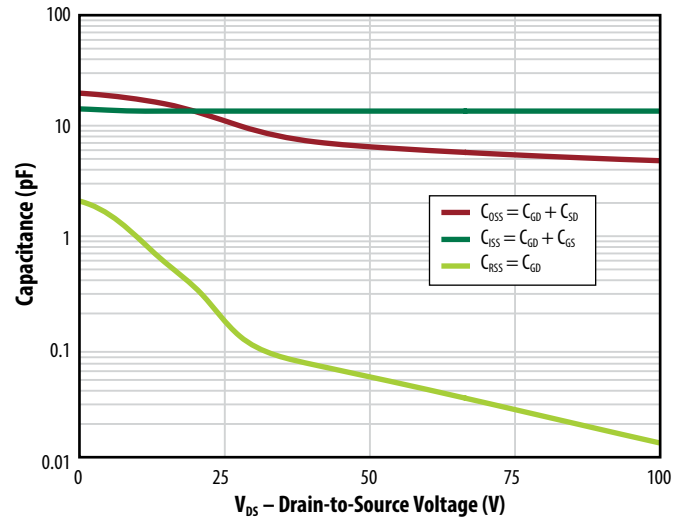


Figure 6: Gate Charge

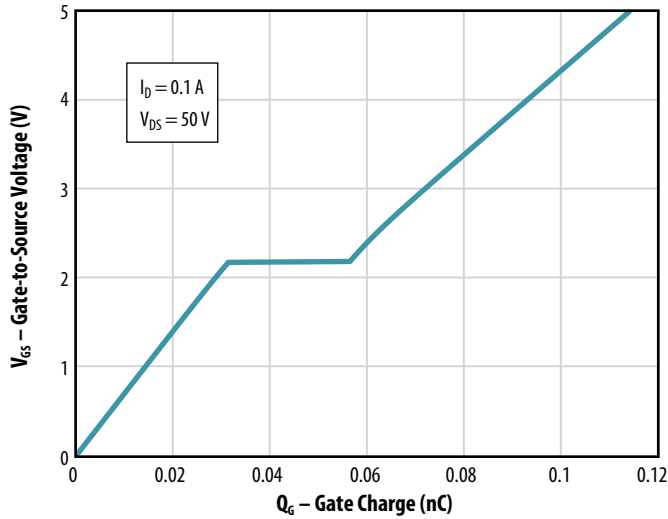


Figure 7: Reverse Drain-Source Characteristics

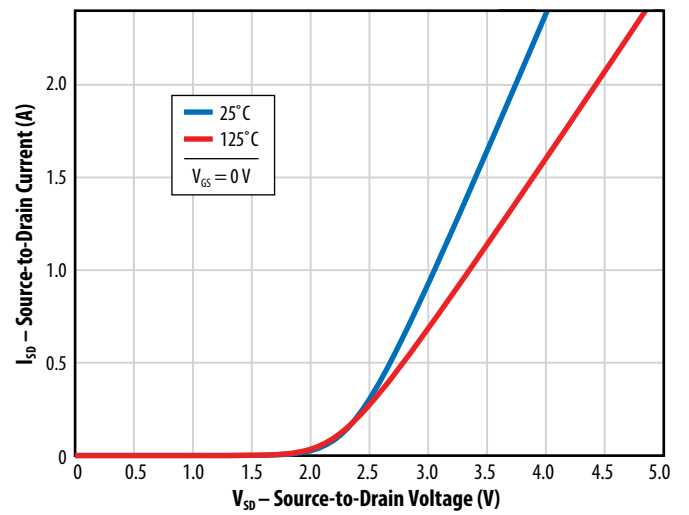


Figure 8: Normalized On-State Resistance vs. Temperature

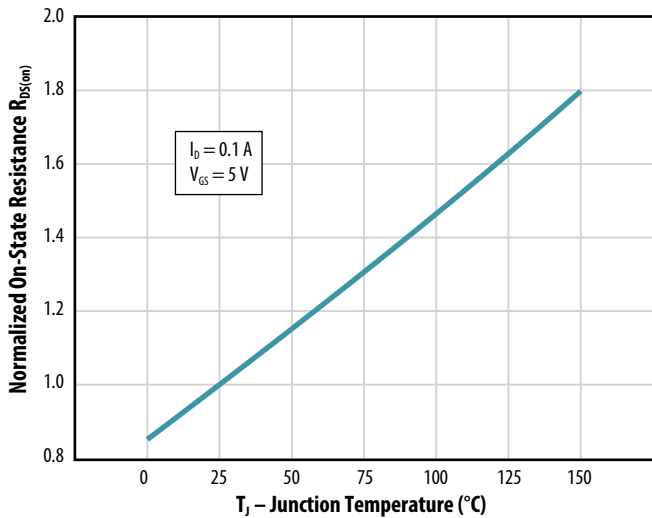


Figure 9: Normalized Threshold Voltage vs. Temperature

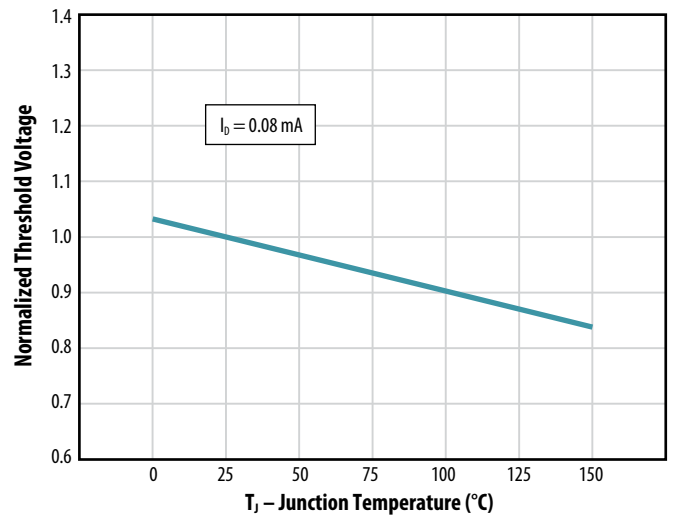


Figure 10: Safe Operating Area

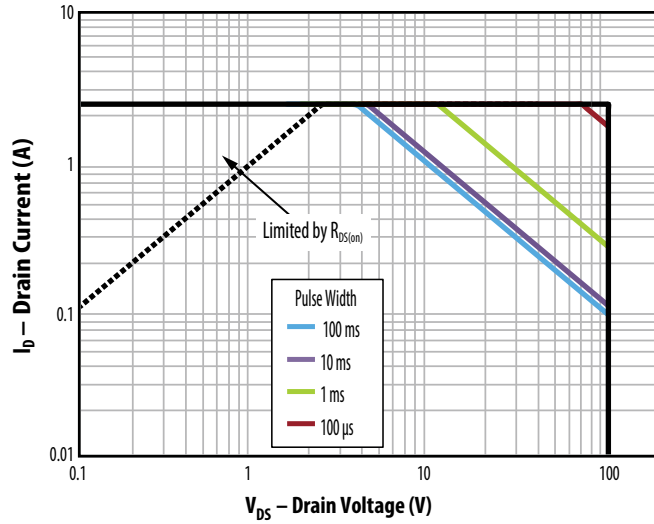
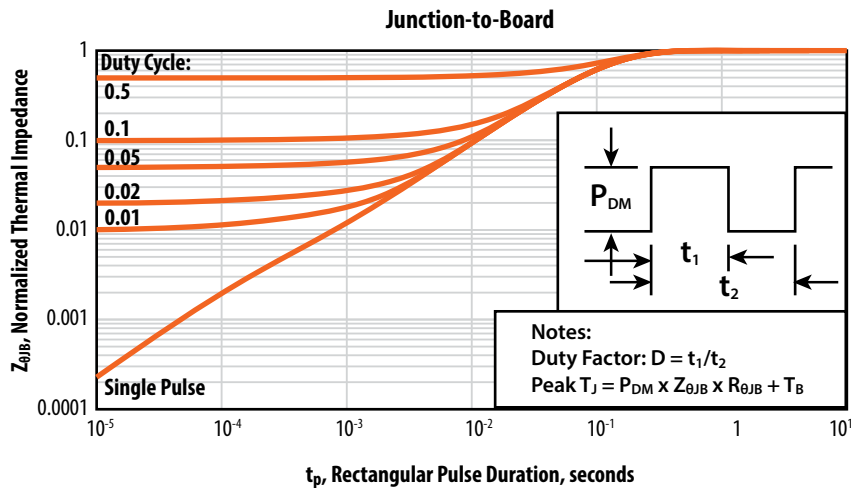
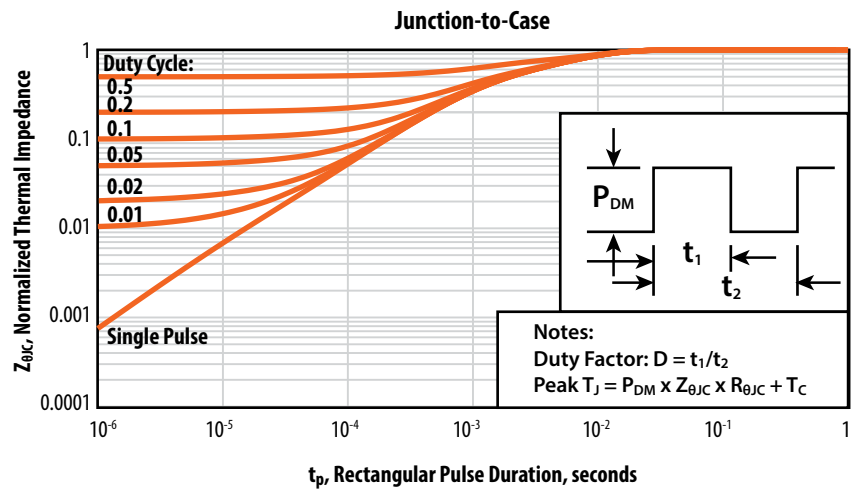
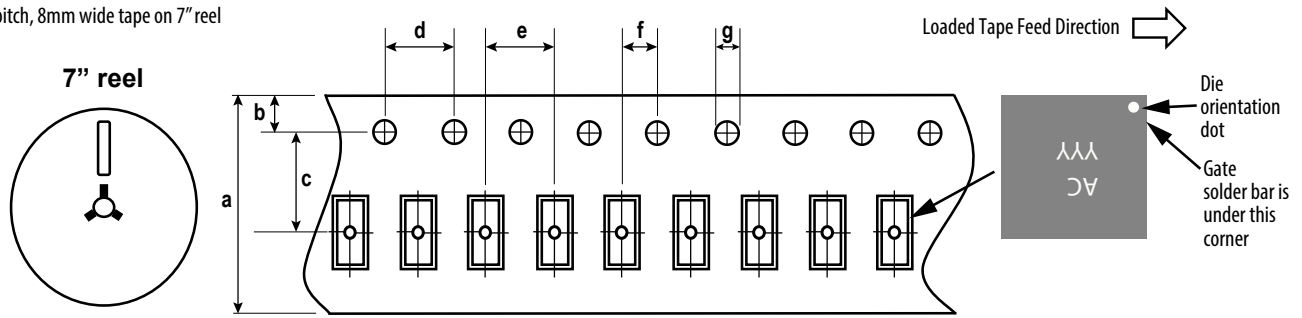


Figure 11: Transient Thermal Response Curves



TAPE AND REEL CONFIGURATION

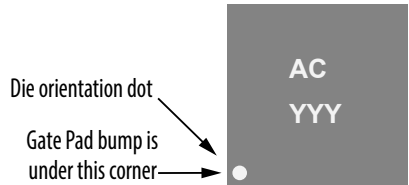
4mm pitch, 8mm wide tape on 7" reel



Dimension (mm)	EPC2037 (note 1)		
	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

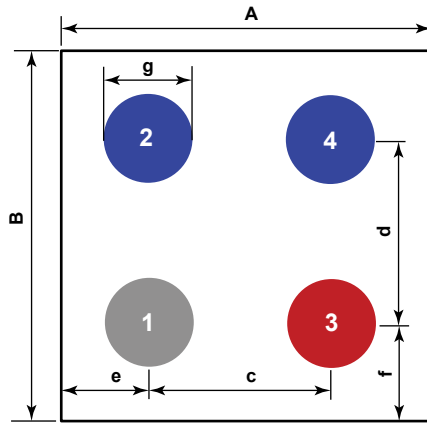
Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
 Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

DIE MARKINGS



Part Number	Laser Markings	
	Part # Marking Line 1	Lot_Date Code Marking line 2
EPC2037	AC	YYY

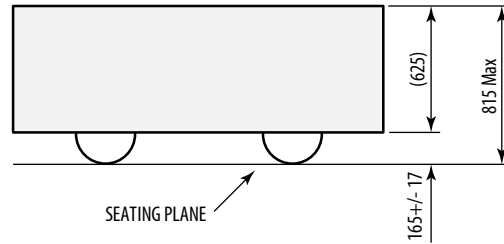
DIE OUTLINE
Solder Bump View



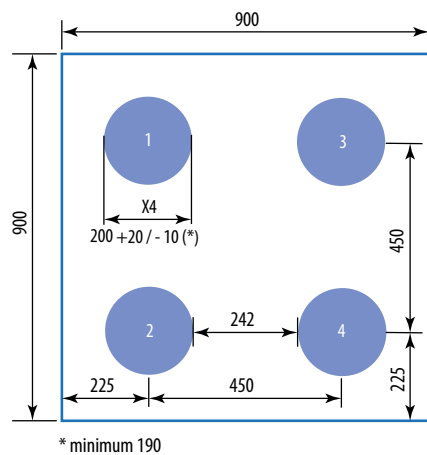
Pad 1 is Gate;
Pad 3 is Drain;
Pads 2, 4 are Source

DIM	MIN	Nominal	MAX
A	870	900	930
B	870	900	930
c	450	450	450
d	450	450	450
e	210	225	240
f	210	225	240
g	187	208	229

Side View



RECOMMENDED LAND PATTERN
(measurements in μm)

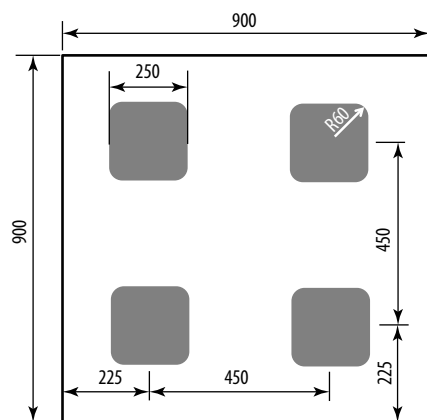


* minimum 190

The land pattern is solder mask defined
Solder mask is 10 μm smaller per side than bump

Pad 1 is Gate;
Pad 3 is Drain;
Pads 2, 4 are Source

RECOMMENDED STENCIL DRAWING
(measurements in μm)



Recommended stencil should be 4mil (100 μm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at
<http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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Information subject to change without notice.

Revised May, 2018