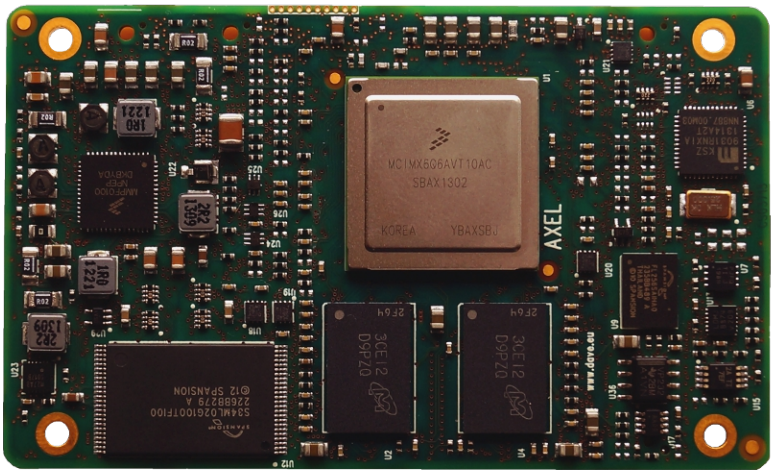
AXEL ULTRA

Solo / Dual / Quad
ARM Cortex-A9 MPCore
CPU Module

ULTRA Line

HARDWARE MANUAL



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1 Preface

1.1 About this manual

This Hardware Manual describes the AXEL CPU module design and functions.
Precise specifications for the NXP/Freescale i.MX6 processor can be found in the CPU datasheets and/or reference manuals.

1.2 Copyrights/Trademarks

1.3 Standards

DAVE Embedded Systems is certified to ISO 9001 standards.

1.4 Disclaimers

DAVE Embedded Systems does not assume any responsibility about availability, supplying and support regarding all the products mentioned in this manual that are not strictly part of the AXEL CPU module.
AXEL CPU Modules are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. **DAVE Embedded Systems** customers who are using or selling these products for use in such applications do so at their own risk and agree to fully indemnify **DAVE Embedded Systems** for any damage resulting from such improper use or sale.

1.5 Warranty

AXEL is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, **DAVE Embedded Systems** will at its discretion decide to repair or replace defective products. Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.
The warranty does not apply to defects resulting from improper or

inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.
DAVE Embedded Systems will not be responsible for any defects or damages to other products not supplied by **DAVE Embedded Systems** that are caused by a faulty AXEL module.

1.6 Technical Support

We are committed to making our product easy to use and will help customers use our CPU modules in their systems. Technical support is delivered through email to our valued customers. Support requests can be sent to support-axel@dave.eu.
Software upgrades are available for download in the restricted access download area of **DAVE Embedded Systems** web site: http://www.dave.eu/reserved-area. An account is required to access this area and is provided to customers who purchase the development kit (please contact support-axel@dave.eu for account requests)..
Please refer to our Web site at http://www.dave.eu/dave-cpu-module-imx6-axel.html for the latest product documentation, utilities, drivers, Product Change Notifications, Board Support Packages, Application Notes, mechanical drawings and additional tools and software.

1.7 Related documents

Document	Location
DAVE Embedded Systems Developers Wiki	http://wiki.dave.eu/index.php/Main_Page
NXP/Freescale i.MX6 Dual/ 6Quad Applications Processor Reference Manual	http://cache.freescale.com/files/32bit/doc/ref_manual/IMX6DQRM.pdf?fpsp=1&WT_TYPE=Reference%20Manuals&WT_VENDOR=FREESCALE&WT_FILE_FORMAT=pdf&WT_ASSET=Documentation

Tab. 1: Related documents

1.8 Conventions, Abbreviations, Acronyms

Abbreviation	Definition
i.MX6 APRM	i.MX6 Application Processor Reference Manual
IPU	Image Processing Unit
GPI	General purpose input
GPIO	General purpose input and output
GPO	General purpose output
PCB	Printed circuit board
RTC	Real time clock
SOM	System on module
TRM	Technical Reference Manual
XELK	AXEL Embedded Linux Kit

Tab. 2: Abbreviations and acronyms used in this manual

Revision History

Version	*Date*	*Notes*
0.9.0	October 2013	First Draft
1.0.0	November 2013	First official release with XELK 1.0.0
1.0.1	January 2014	Minor fixes
1.0.2	August 2014	Minor fixes Fixed power-up sequence diagram
1.0.3	November 2014	Minor fixes Released with XELK 2.0.0
1.0.4	April 2015	Minor fixes Added BOARD_PGOOD info Notes on NVCC_EIM_EXT Released with XELK 2.1.0
1.0.5	September 2016	Minor fixes

2 Introduction

AXEL is the new top-class Solo/Dual/Quad core ARM Cortex-A9 CPU module by **DAVE Embedded Systems**, based on the recent NXP/Freescale i.MX6 application processor.

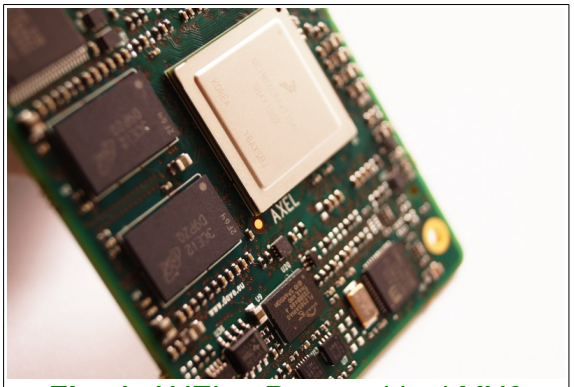


Fig. 1: AXEL – Powered by i.MX6 processor

Thanks to **AXEL**, customers have the chance to save time and resources by using a compact solution that permits to reach scalable performances that perfectly fits the application requirements avoiding complexities on the carrier board.

The use of this processor enables extensive system-level differentiation of new applications in many industry fields, where high-performance and extremely compact form factor (85mm x 50mm) are key factors. Smarter system designs are made possible, following the trends in functionalities and interfaces of the new, state-of-the-art embedded products. **AXEL** offers great computational power, thanks to the rich set of peripherals, the Scalable ARM Cortex-A9 together with a large set of high-speed I/Os (up to 5GHz).

AXEL enables designers to create smart products suitable for harsh mechanical and thermal environments, allowing the development of high computing and reliable solutions. Thanks to the tight integration between the ARM Core-based processing system, designers are able to share the application through the multicore platform and/or to divide the task on different cores in order to match with specific application requirements (AMP makes possible the creation of applications where RTOS and Linux work together on different cores).Thanks to **AXEL**, customers are going to save time and resources by using a powerful and scalable compact solution, avoiding complexities on the carrier PCB.

AXEL is designed and manufactured according to **DAVE Embedded Systems ULTRA Line** specifications, in order to guarantee premium quality and technical value for customers who require top performances and flexibility. **AXEL** is suitable for high-end applications such as medical

instrumentation, advanced communication systems, critical real-time operations and safety applications.

2.1 Product Highlights

- Unmatched performances thanks to Solo / Dual / Quad Core @ 1.2 GHz
- All memories you need on-board
- Boot from NOR for safe applications
- Enabling massive computing applications thanks to wide range DDR3 RAM memory up to 4GB
- Wide range PSU input from 2.8V to 4.5V
- High mechanical retention - 100G shock - thanks to 3x140pins and 4 screw holes
- Reduced carrier complexity: dual CAN, USB, Ethernet GB, PCIe, SATA and native 3.3V I/O
- Suitable for Asymmetric Multicore Processing
- A timing application thanks to on-board 5ppm RTC

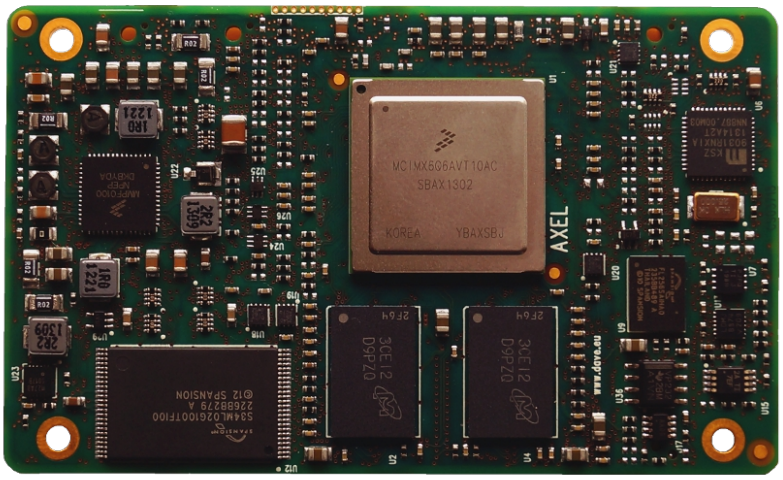
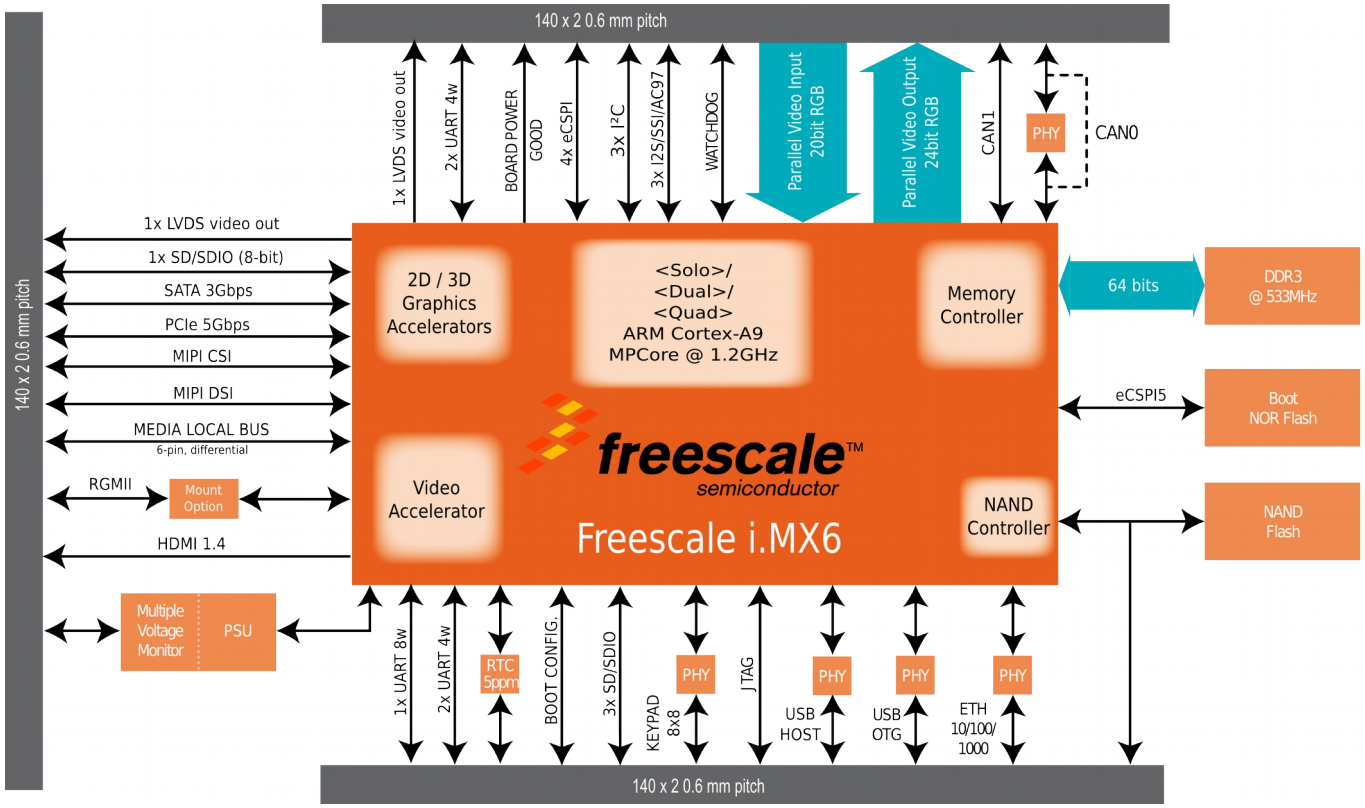


Fig. 2: AXEL SOM (top view)

2.2 Block Diagram



2.3 Feature Summary

Feature	Specifications	Options
CPU	NXP/Freescale i.MX6 ARM Cortex A9 MPCore™ Solo, Dual or Quad core @ 1.2 GHz	
Cache	L1: 32Kbyte instruction, 32Kbyte data L2: Unified instruction and data, 1MByte	
RAM	DDR3 SDRAM @ 533 MHz Up to 4 GB, x64 data bus width	
Storage	Flash NOR SPI (8, 16, 32, 64 MB) Flash NAND (all sizes, on request)	
Expansion bus	One PCI Express 2.0 lane with integrated PHY (5.0 GT/s Endpoint/Root Complex operations)	

Tab. 3: CPU, Memories, Buses

Feature	Specifications	Options
Graphics Controller	16-/24-bit HD Display Port 1x HDMI 1.3 channel + DDC 1x TFT/RGB output port 1x MIPI DSI port 2x LVDS output ports	
2D/3D Engines	GPU2D cores for raster (R2D, Vivante GC320) and vector (V2D, Vivante GC355) graphics acceleration GPU3D core (Vivante GC2000) for OpenGL/OpenGL ES/OpenVG/OpenCL API acceleration	
Video capture	1x 20bit video input 1x MIPI CSI port	
Video processing	High performance, multi-standard VPU Up to 1080p60 H264 decode Up to 1080p30 H264 encode	
Coprocessors	Media Processing Engine with NEON™ & VFPv3-D32 Floating-Point Unit	
USB	1x USB OTG 2.0 with integrated PHY 1x USB Host 2.0 with integrated PHY	
UARTs	5x UART ports (1x full, 4x four-wires)	
GPIO	Up to 206 lines, shared with other functions	

Feature	Specifications	Options
	(interrupts available)	
Networks	Gigabit Ethernet 10/100/1000 Mbps with integrated PHY	
CAN	2x CAN 2.0B ports (1x with integrated PHY)	
SD/MMC	4x SD 3.0 /SDIO 3.0/MMC 4.x compliant controllers	
Storage	Serial ATA II 3.0 Gbps with integrated PHY	
Serial buses	5x full-duplex SPI ports with four peripheral chip selects 3x master and slave I²C interfaces	
Audio	3x I²S/SSI/AC97 interfaces	
Timers	Enhanced Periodic Interrupt Timer General Purpose Timer	
RTC	On board, ±3.5ppm (DS3232), external battery powered	
Watchdog	On board, configurable timeout (MAX6373)	
Debug	JTAG IEEE 1149.1 Test Access Port CoreSight™ and Program Trace Macrocell (PTM)	

Tab. 4: Peripherals

Feature	Specifications	Options
Supply Voltage	2.8-4.5V wide range input, voltage regulation on board	
Active power consumption	See section 8.3 - Power consumption	
Dimensions	85mm x 50mm	
Weight	<tbd>	
MTBF	<tbd>	
Operating temperature range	Commercial: 0°C / +70°C Industrial: -40°C / +85°C	
Shock	100 G	
Vibration	<tbd>	
Connectors	3 x 140 pins 0.6mm pitch	
Connectors	<tbd>	

Feature	Specifications	Options
insertion / removal		

Tab. 5: Electrical, Mechanical and Environmental Specifications

3 Design overview

The heart of AXEL module is composed by the following components:

- NXP/Freescale i.MX6 Solo / Dual / Quad core SoC application processor
- Power supply unit
- DDR memory banks
- NOR and NAND flash banks
- 3x 140 pin connectors with interfaces signals

This chapter shortly describes the main AXEL components.

3.1 NXP/Freescale i.MX6 application processor

The i.MX6 Solo/Dual/Quad processors feature NXP/Freescale's advanced implementation of the ARM® Cortex®-A9 MPCore, which operates at speeds up to 1.2 GHz. They include 2D and 3D graphics processors, 1080p video processing, and integrated power management. As a result, the i.MX6 devices are able to serve a wide range of applications including:

- Automotive driver assistance, driver information, and infotainment
- Multimedia-centric smart mobile devices
- Instrument clusters, and portable medical devices.
- E-Readers, smartbooks, tablets
- Intelligent industrial motor control, industrial networking, and machine vision
- IP and Smart camera
- Human-machine interfaces
- Medical diagnostics and imaging
- Digital signage
- Video and night vision equipment
- Multimedia-focused products
- Entertainment and gaming appliances

The i.MX6 application processor is composed of the following major functional blocks:

- ARM Cortex-A9 MPCore 2x/4x CPU Processor, featuring:
  - 1 Megabyte unified L2 cache shared by all CPU cores
  - NEON MPE coprocessor
  - General Interrupt Controller (GIC) with 128 interrupt support
  - Snoop Control Unit (SCU)
  - External memories interconnect
- Hardware accelerators, including:
  - VPU -Video Processing Unit
  - Two IPUv3H -Image Processing Unit (version 3H)
  - 2D/3D/Vector graphics accelerators
- Connectivity peripherals, including
  - PCIe
  - SATA
  - SD/SDIO/MMC
  - Serial buses: USB, UART, I^2C, SPI, ...

AXEL can mount three versions of the i.MX6 processor. The following table shows a **comparison** between the processor models, highlighting the differences:

Processor	# cores	Clock	L2 cache	DDR3	Graphics acceleration	IPU	VPU	SATA-II
i.MX6 Solo	1	800 MHz 1 GHz	512 KB	32 bit @ 400 MHz	*3D*: Vivante GC880 *2D*: Vivante GC320 *Vector*: N.A.	1x	1x	N.A.
i.MX6 Dual	2	850 MHz 1 GHz 1.2 GHz	1 MB	64 bit @ 533 MHz	*3D*: Vivante GC2000 *2D*: Vivante GC320 *Vector*: Vivante GC335	2x	2x	Yes
i.MX6 Quad	4	850 MHz 1 GHz 1.2 GHz	1MB	64 bit @ 533 MHz	*3D*: Vivante GC2000 *2D*: Vivante GC320 *Vector*: Vivante GC335	2x	2x	Yes

Tab. 6: i.MX6 comparison

3.2 DDR3 memory bank

DDR3 SDRAM memory bank is composed by 4x 16-bit width chips resulting in a 64-bit combined width bank.
The following table reports the SDRAM specifications:

CPU connection	Multi-mode DDR controller (MMDC)
Size min	512 MB
Size max	4 GB
Width	64 bit
Speed	533 MHz

Tab. 7: DDR3 specifications

3.3 NOR flash bank

NOR flash is a Serial Peripheral Interface (SPI) device. This device is connected to the eCSPI channel 5 and by default it acts as boot memory.
The following table reports the NOR flash specifications:

CPU connection	eCSPI channel 5
Size min	8 MByte
Size max	64 MByte
Chip select	ECSPI5_SS0
Bootable	Yes

Tab. 8: NOR flash specifications

3.4 NAND flash bank

On board main storage memory is a 8-bit wide NAND flash connected to the CPU's Raw NAND flash controller. Optionally, it can act as boot peripheral.
The following table reports the NAND flash specifications:

CPU connection	Raw NAND flash controller
Page size	512 byte, 2 kbyte or 4 kbyte
Size min	128 MByte
Size max	2 GByte
Width	8 bit
Chip select	NANDF_CS0
Bootable	Yes

Tab. 9: NAND flash specifications

3.5 Memory Map

For detailed information, please refer to chapter 2 “Memory Maps” of the i.MX Applications Processor Reference Manual.

3.6 Power supply unit

AXEL, as the other ULTRA Line CPU modules, embeds all the elements required for powering the unit, therefore power sequencing is self-contained and simplified. Nevertheless, power must be provided from carrier board, and therefore users should be aware of the ranges power supply can assume as well as all other parameters. For detailed information, please refer to Section 5.1.

3.7 CPU module connectors

All interface signals AXEL provides are routed through three 140 pin 0.6mm pitch stacking connectors (named J1, J2 and J3). The dedicated carrier board must mount the mating connectors and connect the desired peripheral interfaces according to AXEL pinout specifications.
For mechanical information, please refer to Section 4 (Mechanical specifications). For pinout and peripherals information, please refer to Sections 6 (Pinout table) and 7 (Peripheral interfaces).

4 Mechanical specifications

This chapter describes the mechanical characteristics of the AXEL module.

Mechanical drawings are available in DXF format from the AXEL page on DAVE Embedded Systems website (http://www.dave.eu/products/som/freescale/imx6_axel-ultra).

4.1 Board Layout

The following figure shows the physical dimensions of the AXEL module:

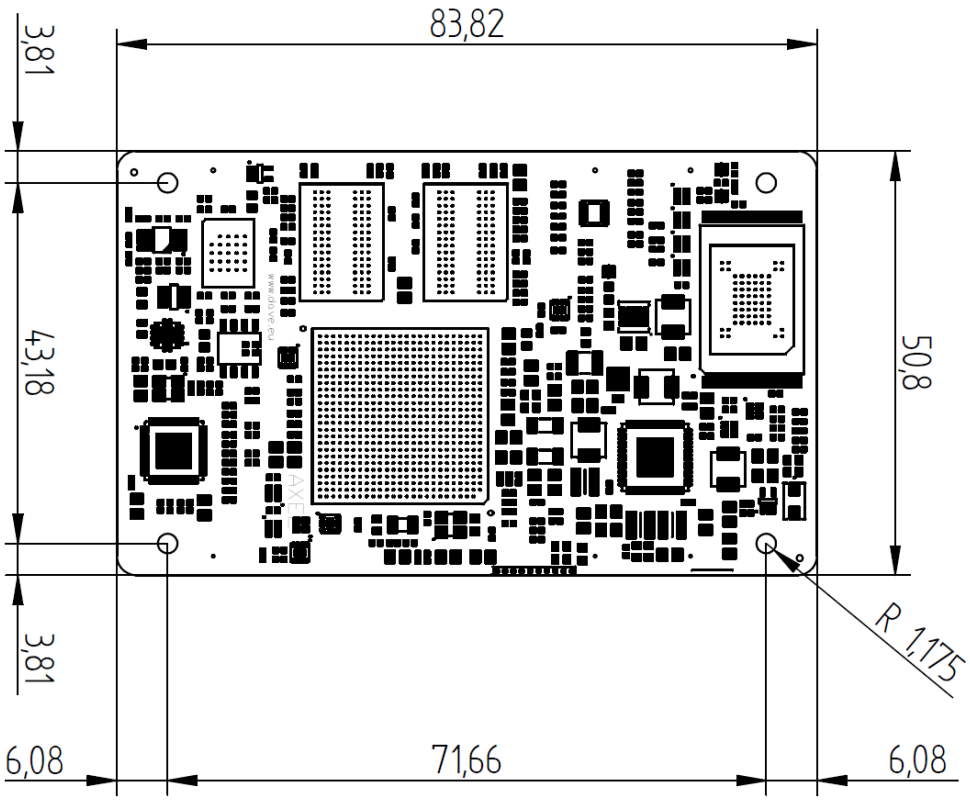


Fig. 3: Board layout - Top view

- Board height: 50.8 mm

- Board width: 83.8 mm
- Maximum components height is 2 mm (top) and 4 mm (bottom)
- PCB thickness is 1.9 mm

The following figure highlights the maximum components' heights on AXEL module:

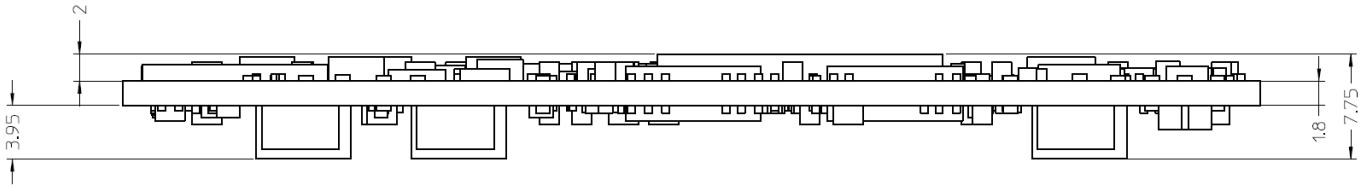


Fig. 4: Board layout - Side view

4.2 Connectors

The following figure shows the AXEL connectors layout:

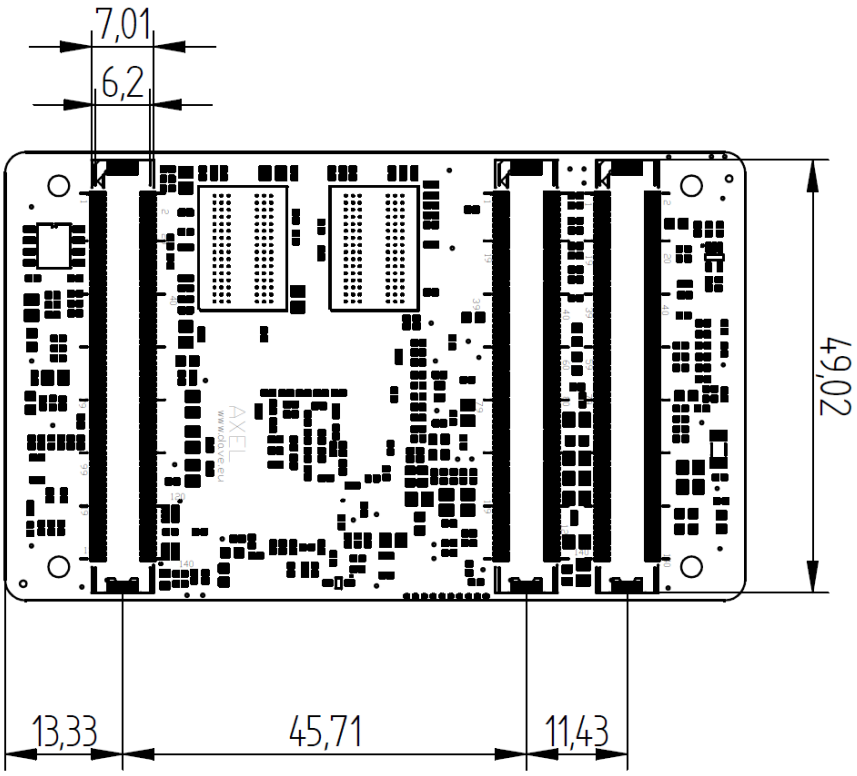


Fig. 5: Connectors layout

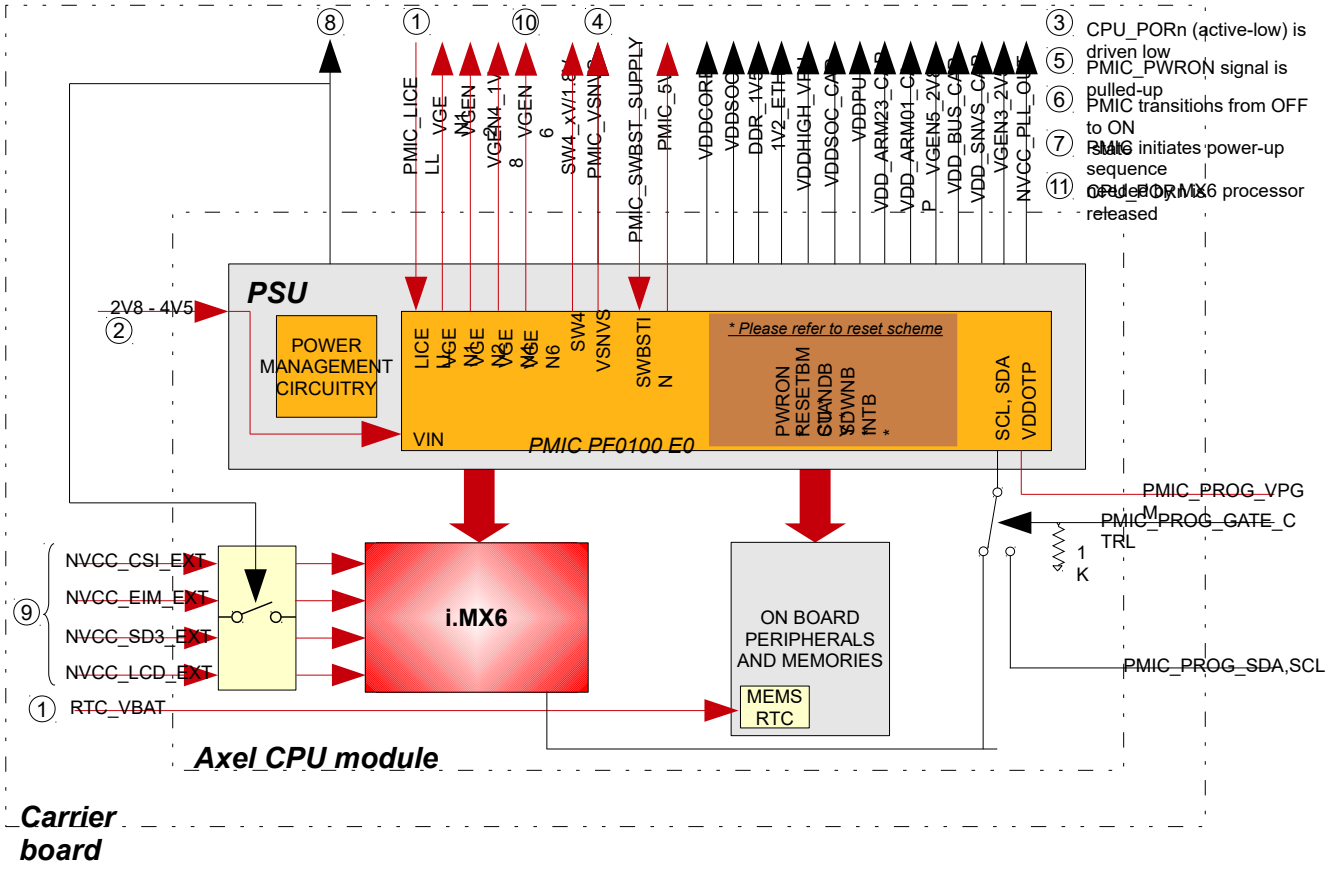
The following table reports connectors specifications:

Part number	Hirose FX8C-140S-SV
Height	5.1 mm
Length	48.6 mm
Depth	4.0 mm
Mating connectors	Hirose FX8C-140P-SV (5 mm board-to-board height) Hirose FX8C-140P-SV1 (6 mm board-to-board height) Hirose FX8C-140P-SV2 (7 mm board-to-board height) Hirose FX8C-140P-SV4 (9 mm board-to-board height) Hirose FX8C-140P-SV6 (11 mm board-to-board height)

5 Power, reset and control

5.1 Power Supply Unit (PSU) and recommended power-up sequence

Implementing correct power-up sequence for i.MX6 processors is not a trivial task because several power rails are involved. AXEL SOM simplifies this task and embeds all the needed circuitry. The following picture shows a simplified block diagram of PSU/voltage monitoring circuitry:



The PSU is composed of two main blocks:

- power management integrated circuit (PMIC, NXP/Freescale PF0100E0 - on request this part is available in automotive grade)
- additional generic power management circuitry that completes PMIC functionalities.

The PSU:

- generates the proper power-up sequence required by i.MX processor and surrounding memories and peripherals
- synchronizes the powering up of carrier board in order to prevent back power
- provides some spare regulated voltages that can be used to power carrier board devices

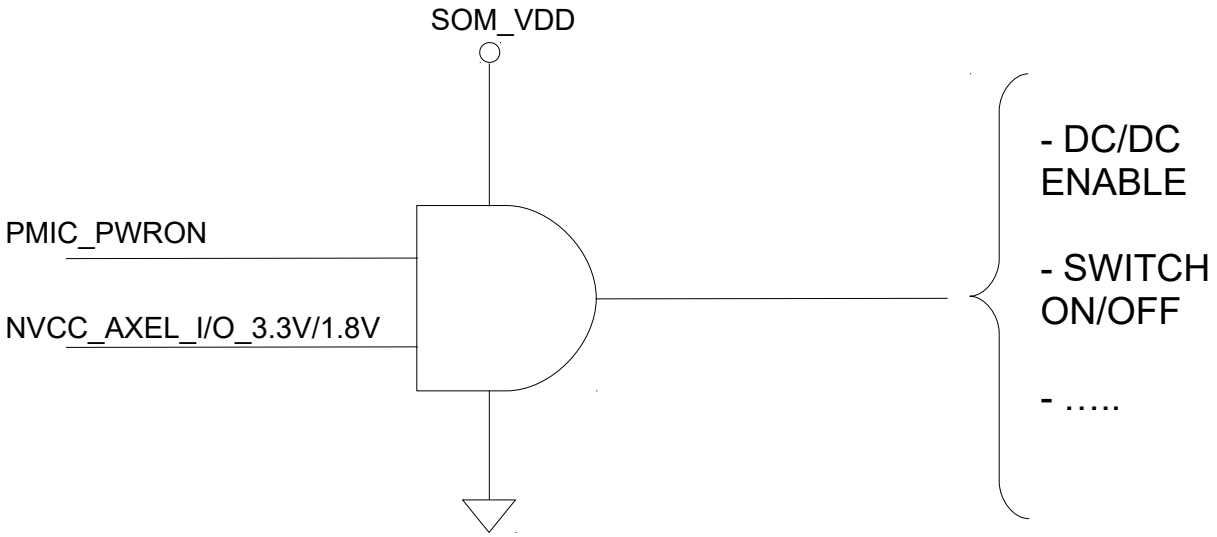
The typical power-up sequence is the following:

1. (optional) PMIC_LICELL is powered
   (optional) RTC_VBAT is powered
2. 2V8-4V5 main power supply rail is powered
3. CPU_PORn (active-low) is driven low
4. PMIC activates PMIC_VSNVS power output
5. PMIC_PWRON signal is pulled-up (unless carrier board circuitry keeps this signal low for any reason)
6. PMIC transitions from OFF to ON state
7. PMIC initiates power-up sequence needed by MX6 processor
8. NVCC_AXEL_I/O_3.3V/1.8V signal is raised; this active-high signal indicates that SoM's I/O is powered. This signal can be used to manage carrier board power up sequence in order to prevent back powering (from SoM to carrier board or vice versa)
9. configurable I/O power rails (NVCC_CSI_EXT, NVCC_EIM_EXT, NVCC_SD3_EXT, NVCC_LCD_EXT) are powered by carrier board
10. PMIC VGEN6 LDO is turned on (this is the last regulator turned on automatically by PMIC)

11. CPU_PORn is released.

5.1.1 Note on NVCC_AXEL_I/O_3.3V/1.8V (BOARD_PGOOD) usage

NVCC_AXEL_I/O_3.3V/1.8V is generally used on carrier board to drive loads such as DC/DC enable inputs or switch on/off control signals. Depending on the kind of such loads, NVCC_AXEL_I/O_3.3V/1.8V might not be able to drive them properly. In these cases a simple 2-input AND port can be used to address this issue. The following picture depicts a principle schematic showing this solution. VDD_SOM denotes the power rail used to power AXEL ULTRA SoM.



5.1.2 Note on NVCC_EIM_EXT

If the SPI NOR flash is mounted on the AXEL ULTRA SoM, the NVCC_EIM_EXT input signal can't be configured as an extended range voltage, but it must be connected to a +3.3V rail (because the SPI bus used internally for the NOR flash shares some pins of the EIM bank).

5.1.3 Power rails and related signals

The following list describes in detail power rails and power related signals. **Please note that PMIC regulators ouput voltages can be changed only if explicitly allowed.**

- 2V8-4V5: this is external main power rail. Voltage range is 2.8 - 4.5V
- PMIC_CELL: PMIC's coin cell supply input/output

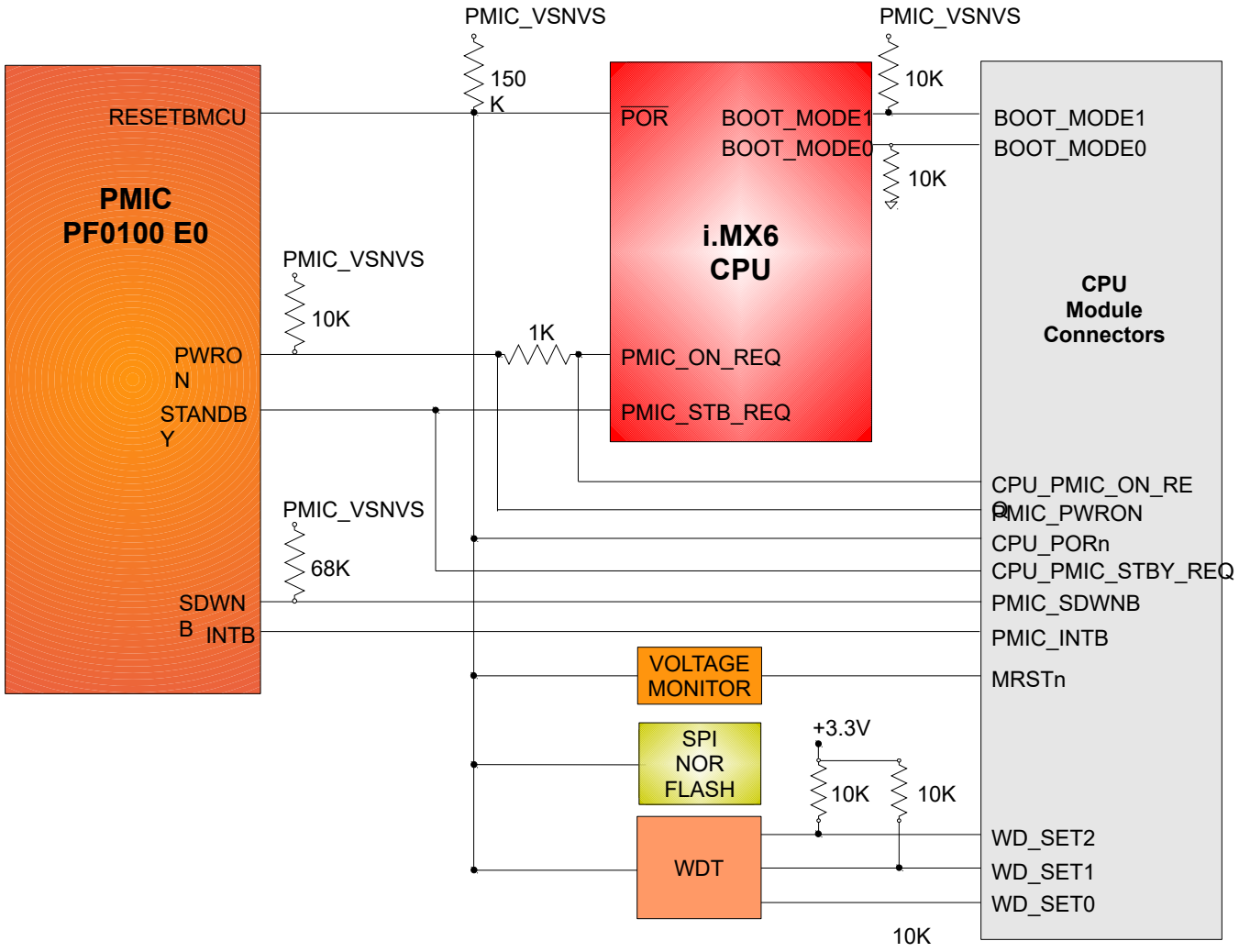
- RTC_VBAT: this rail is connected to pin 6 of Maxim DS3232MZ+ RTC
- NVCC_CSI_EXT: this rail powers MX6's NVCC_CSI domain
- NVCC_EIM_EXT: this rail powers MX6's NVCC_EIM0, NVCC_EIM1 and NVCC_EIM2 domains
- NVCC_SD3_EXT: this rail powers MX6's NVCC_SD3 domain
- NVCC_LCD_EXT: this rail powers MX6's NVCC_LCD domain
- NVCC_AXEL_I/O_3.3V/1.8V: this output signal is used to indicate when carrier board's circuitry interfacing AXEL's I/Os has to be powered up
- VGEN1: PMIC's VGEN1 regulator output; this regulator is not used by any AXEL's internal load. Output voltage can be selected by user.
- VGEN2: PMIC's VGEN2 regulator output; this regulator is not used by any AXEL's internal load. Output voltage can be selected by user.
- VGEN4_1V8: PMIC's VGEN4 regulator output; output voltage (1.8V) must not be altered. Up to 150mA can be drawn.
- VGEN6: PMIC's VGEN6 regulator output; this regulator is not used by any AXEL's internal load. Output voltage can be selected by user.
- SW4_xV/1.8V: PMIC's SW4 regulator output voltage (1.8V). This voltage must not be altered. Up to 500mA can be drawn.
- PMIC_VSNVS: PMIC's LDO or coin cell output to processor. Please refer to PMIC's datasheet for current limit. Please take into account internal loads as depicted in AXEL reset scheme picture.
- PMIC_SWBST_SUPPLY: this rail is connected to PMIC's SWBSTIN pad and can be used to power SWBST boost regulator. This regulator is not used by any AXEL's internal load. Output voltage can be selected by user.
- PMIC_5V: this is output of SWBST boost regulator. This regulator is not used by any AXEL's internal load. Output voltage can be selected by user.
- VDDCORE, VDDSOC, DDR_1V5, 1V2_ETH, VDDHIGH_VPH, VDDSOC_CAP, VDDPU, VDD_ARM23_CAP, VDD_ARM01_CAP,

VDGEN5_2V8, VDD_BUS_CAP, VDD_SNVS_CAP, VGEN3_2V5, NVCC_PLL_OUT: these signals route power voltage generated by AXEL PSU. These optional signals (in the default configuration, the pins are dedicated to other functions) are meant to enable monitoring of internal voltages by carrier board circuitry. For further details, please refer to pinout table.

For further details, please refer to the PMIC documentation:
http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MMPF0100%7CPF0100

5.2 Reset scheme and control signals

The following picture shows the simplified block diagram of reset scheme and voltage monitoring.



The available reset signals are described in detail in the following sections.

5.2.1 CPU_PORn

The following sources can assert this active-low signal:

- PMIC
- multiple-voltage monitor: this device monitors several critical power voltages and triggers a reset pulse in case any of these exhibits a brownout condition
- MRSTn: this signal is connected to the RESET IN input of the voltage monitor. MRSTn is pulled-up to processor's I/O voltage with 2.2 kOhm resistor.
- watchdog timer: even if MX6 processor integrates a watchdog timer (WDT), an external WDT (Maxim MAX6373KA+) is avalible to maximize reliability

Since SPI NOR flash can be used as boot device, CPU_PORn is connected to this device too. This guarantees it is in a known state after reset occurrence.

5.2.2 Boot_Mode0/1

By default, BOOT_MODE0 is pulled-down with 10kOhm resistor and BOOT_MODE1 is pulled-up to PMIC_VSNVS with 10kOhm resistor. Different configurations are available on request. For further details, please refer to section 5.4.2.

5.3 Voltage monitor

The voltage monitor is a Linear Technology LTC2930 (Configurable Six Supply Monitor with Adjustable Reset Timer, Manual Reset).

5.4 System boot

The boot process begins at Power On Reset (POR) where the hardware reset logic forces the ARM core to begin execution starting from the on-chip boot ROM. Boot ROM code uses the state of the internal register BOOT_MODE[1:0] as well as the state of various eFUSEs and/or GPIO settings to determine the boot flow behavior of the device. The boot ROM:

- determines whether the boot is secure or non-secure
- performs some initialization of the system and clean-ups
- reads the mode pins to determine the primary boot device
- once it is satisfied, it executes the boot code

5.4.1 Boot modes

The boot ROM supports the following boot devices:

- NOR Flash
- NAND Flash
- OneNAND Flash
- SD/MMC
- Serial ATA HDD (only on i.MX6 Dual/Quad)
- Serial (I2C/SPI) NOR Flash and EEPROM

Boot mode is selectable via two mode pins (BOOT_MODE[1:0]), and 32 boot configuration signals, (BOOT_CFGx[7:0], x=1,2,3,4). The pins are used as follows:

Function	Boot signals	Available options
Boot mode selection	BOOT_MODE[1:0]	00: Boot from fuses 01: Serial downloader 10: Internal Boot 11: Reserved
L1 I Cache disable bit	BOOT_CFG3[7]	0: L1 I Cache is enabled by ROM during the boot 1: L1 I Cache is disabled by ROM during the boot
MMU/L1 D Cache/PL310 disable bit	BOOT_CFG3[6]	0: MMU/L1 D Cache/PL310 is enabled by ROM during the boot 1: MMU/L1 D Cache/PL310 is disabled by ROM during the boot
Frequency Selection	BOOT_CFG3[2]	0: ARM - 792MHz, DDR - 532MHz, AXI - 264MHz 1: ARM - 396MHz, DDR - 352MHz, AXI - 176MHz
Boot Configuration1	BOOT_CFG1[7:0]	Specific to selected boot mode
Boot Configuration2	BOOT_CFG2[7:0]	Specific to selected boot mode
Infinite Loop Enable at start of boot ROM	BOOT_CFG4[7]	0: Disabled 1: Enabled
Boot	BOOT_CFG4[6:0]	Specific to selected boot

Function	Boot signals	Available options
Configuration4		mode

Boot device selection is specified by BOOT_CFG1[7:3] pins, as described on the table below:

Boot device	Boot signals BOOT_CFG[7:3]	i.MX6 APRM pin map reference
EIM	00000 – NOR flash 00001 - OneNAND	Table 5.4 (page 352)
SATA	0010X[1]	Table 5.5 (page 354)
Serial ROM	0011X[1]	Table 5.6 (page 355)
SD/eSD	010XX[1]	Table 5.7 (page 356)
MMC/eMMC	011XX[1]	Table 5.8 (page 358)
NAND Flash	1XXXX[1]	Table 5.9 (page 359)

In order to fully understand how boot works on AXEL platform, please refer to chapter 8 ("System boot") of the i.MX6 APRM.

5.4.2 Default boot configuration

Default configuration for AXEL module is to boot from SPI NOR flash, connected to eCSPI5 channel (SS0 chip select) with 3 Byte address mode. This is achieved with the following bit mapping:

- BOOT_MODE[1:0] = 10b: Internal mode
- BOOT_CFG1[7:0] = 00110011b:
- BOOT_CFG2[7:0] = 11011101b
- BOOT_CFG3[7:0] = 11001000b
- BOOT_CFG4[7:0] = 01001100b

The boot code performs hardware initialization, loads the U-Boot bootloader image (Program Image) from the chosen boot device and then jumps to an address derived from the Program Image. If any error occurs during internal boot, the boot code jumps to the Serial Downloader (please refer to section 5.6.2).

1 X: please refer to the device specific BOOT_CFG pin map on the i.MX6 APRM

5.4.3 Boot sequence customization

BOOT_CFG pins are routed to the J2 connector, enabling for the customization of the boot sequence through a simple resistor network that can be implemented on carrier board hosting AXEL module.

Mode signal	J2 pin	Pin name
BOOT_CFG1[0]	J2.3	EIM_DA0
BOOT_CFG1[1]	J2.5	EIM_DA1
BOOT_CFG1[2]	J2.7	EIM_DA5
BOOT_CFG1[3]	J2.9	EIM_DA3
BOOT_CFG1[4]	J2.11	EIM_DA4
BOOT_CFG1[5]	J2.13	EIM_DA5
BOOT_CFG1[6]	J2.15	EIM_DA6
BOOT_CFG1[7]	J2.17	EIM_DA7
BOOT_CFG2[0]	J2.19	EIM_DA8
BOOT_CFG2[1]	J2.23	EIM_DA9
BOOT_CFG2[2]	J2.25	EIM_DA10
BOOT_CFG2[3]	J2.27	EIM_DA11
BOOT_CFG2[4]	J2.29	EIM_DA12
BOOT_CFG2[5]	J2.31	EIM_DA13
BOOT_CFG2[6]	J2.33	EIM_DA14
BOOT_CFG2[7]	J2.35	EIM_DA15
BOOT_CFG3[0]	J2.37	EIM_DA16
BOOT_CFG3[1]	J2.39	EIM_DA17
BOOT_CFG3[2]	J2.43	EIM_DA18
BOOT_CFG3[3]	J2.45	EIM_DA19
BOOT_CFG3[4]	J2.47	EIM_DA20
BOOT_CFG3[5]	J2.49	EIM_DA21
BOOT_CFG3[6]	J2.51	EIM_DA22
BOOT_CFG3[7]	J2.53	EIM_DA23
BOOT_CFG4[0]	J2.55	EIM_DA24
BOOT_CFG4[1]	J2.57	EIM_DA25
BOOT_CFG4[2]	J2.59	EIM_DA26
BOOT_CFG4[3]	J2.63	EIM_DA27

Mode signal	J2 pin	Pin name
BOOT_CFG4[4]	J2.65	EIM_DA28
BOOT_CFG4[5]	J2.67	EIM_DA29
BOOT_CFG4[6]	J2.69	EIM_DA30
BOOT_CFG4[7]	J2.71	EIM_DA31

For each BOOT_MODE[31:0] pin it is possible to populate upper or lower side resistor in order to change default value that is set on module itself.

5.5 Clock scheme

This section will be completed in a future version of this manual.

5.6 Recovery

For different reason, starting from image corruption due power loss during upgrade or unrecoverable bug while developing a new U-Boot feature, the user will need, sooner or later, to recover (*bare-metal* restore) the AXEL SOM without using the bootloader itself. The following paragraphs introduce the available options. For further information, please refer to **DAVE Embedded Systems** Developers Wiki or contact the Technical Support Team.

5.6.1 JTAG Recovery

JTAG recovery, though very useful (especially in development or production environment), requires dedicated hardware and software tools. AXEL provides the JTAG interface, which, besides the debug purpose, can be used for programming and recovery operations. For further information on how to use the JTAG interface, please contact the Technical Support Team.

5.6.2 USB Recovery

The USB Serial Downloader provides a means to download the bootloader image to the chip over USB serial connection. Please refer to the XELK Quick Start Guide for further details.

5.6.3 SD/MMC Recovery

MMC recovery is a valuable options that requires no special hardware at all, apart a properly formatted MMC. The boot sequence must include the

SD/MMC option and a way to enable it. When SD/MMC boot option is selected, bootrom looks for a valid FSBL on SD/MMC, which in turn will load the 2nd stage bootloader. Once the board is running after booting from SD, reprogramming the flash memory is straightforward.

5.7 Multiplexing

Most of the i.MX6 processor pins have multiple signal options. These signal to pin and pin to signal options are selected by the input output multiplexer called IOMUX. The IOMUX enables flexible IO multiplexing and is also used to configure other pin characteristics, such as voltage level, drive strength, and hysteresis. Each IO pad has default and up to seven alternate functions, which are software configurable.

Please refer to the following sections of the i.MX6 APRM for further information pin assignment:

- chapter 4 “External Signals and Pin Multiplexing”
- section 4.1 “Pin assignments”
- section 4.2 “Muxing options”
- chapter 36 “IOMUX Controller (IOMUXC)”

5.8 RTC

An on-board Maxim Integrated DS3232 device provides a very accurate, temperature-compensated real-time clock (RTC) resource with:

- Temperature-compensated crystal oscillator
- Date, time and calendar
- Alarm capability
- Backup power from external battery
- ±3.5ppm accuracy from -40°C to +85°C
- 236 Bytes of Battery-Backed SRAM
- I²C Interface

Backup power is provided through the RTC_VBAT (J1.124) signal. If not used, RTC_VBAT must be externally connected to VCC.

For a detailed description of RTC characteristics, please refer to the DS3232 datasheet.

5.9 Watchdog

An external watchdog (Maxim MAX6373) is connected to the PORSTn signal. During normal operation, the microprocessor should repeatedly toggle the watchdog input WDI before the selected watchdog timeout period elapses to demonstrate that the system is processing code properly. If the µP does not provide a valid watchdog input transition before the timeout period expires, the supervisor asserts a watchdog (WDO) output to signal that the system is not executing the desired instructions within the expected time frame. The watchdog output pulse is used to reset the µP. WDI is is available on AXEL connectors as WDT_WDI (J3.117).

The MAX6373 watchdog timer is pin-selectable and the timer can be configured through the WD_SET0 (J1.67), WD_SET1 (J1.69) and WD_SET2 (J1.71) signals. As a default, the watchdog is configured through a pull-up/pull-down resistors network (WD_SET[2..0] = 110) that keeps the watchdog timer inactive at startup. Startup delay ends when WDI sees its first level transition. The default watchdog timeout period is 10 s.

The configuration can be changed by optional external circuitry implemented on the carrier board.

6 Pinout table

This chapter contains the pinout description of the AXEL module, grouped in six tables (two – odd and even pins – for each connector) that report the pin mapping of the three 140-pin AXEL connectors.
Each row in the pinout tables contains the following information:

Pin	Reference to the connector pin
Pin Name	Pin (signal) name on the AXEL connectors
Internal Connections	Connections to the AXEL components: CPU.<x> : pin connected to CPU (PS, processing system) pad named <x> CAN.<x> : pin connected to the CAN transceiver PMIC.<x> : pin connected to the Power Manager IC LAN.<x> : pin connected to the LAN PHY SV.<x>: pin connected to voltage supervisor MTR: pin connected to voltage monitors NOR: pin connected to SPI NOR flash
Ball/pin #	Component ball/pin number connected to signal
Supply Group	Power Supply Group
Type	Pin type: I = Input, O = Output, D= Differential, Z = High impedance, S = Supply voltage, G = Ground, A = Analog signal
Voltage	I/O voltage

6.1 Carrier board mating connector J1

J1 – ODD [1 - 139]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J1.1	DGND	DGND	-				
J1.3	DI0_DISP_CLK	CPU.DI0_DISP_CLK	N19	NVCC_			
J1.5	DI0_PIN2	CPU.DI0_PIN2	N25	NVCC_			
J1.7	DI0_PIN3	CPU.DI0_PIN3	N20	NVCC_			
J1.9	DI0_PIN4	CPU.DI0_PIN4	P25	NVCC_			
J1.11	DI0_PIN15	CPU.DI0_PIN15	N21	NVCC_			
J1.13	DISP0_DAT0	CPU.DISP0_DAT0	P24	NVCC_			
J1.15	DISP0_DAT1	CPU.DISP0_DAT1	P22	NVCC_			
J1.17	DISP0_DAT2	CPU.DISP0_DAT2	P23	NVCC_			
J1.19	DISP0_DAT3	CPU.DISP0_DAT3	P21	NVCC_			
J1.21	DGND	DGND	-				
J1.23	DISP0_DAT4	CPU.DISP0_DAT4	P20	NVCC_			
J1.25	DISP0_DAT5	CPU.DISP0_DAT5	R25	NVCC_			
J1.27	DISP0_DAT6	CPU.DISP0_DAT6	R23	NVCC_			
J1.29	DISP0_DAT7	CPU.DISP0_DAT7	R24	NVCC_			
J1.31	DISP0_DAT8	CPU.DISP0_DAT8	R22	NVCC_			
J1.33	DISP0_DAT9	CPU.DISP0_DAT9	T25	NVCC_			
J1.35	DISP0_DAT10	CPU.DISP0_DAT10	R21	NVCC_			
J1.37	DISP0_DAT11	CPU.DISP0_DAT11	T23	NVCC_			
J1.39	DISP0_DAT12	CPU.DISP0_DAT12	T24	NVCC_			
J1.41	DGND	DGND	-				
J1.43	DISP0_DAT13	CPU.DISP0_DAT13	R20	NVCC_			
J1.45	DISP0_DAT14	CPU.DISP0_DAT14	U25	NVCC_			
J1.47	DISP0_DAT15	CPU.DISP0_DAT15	T22	NVCC_			
J1.49	DISP0_DAT16	CPU.DISP0_DAT16	T21	NVCC_			
J1.51	DISP0_DAT17	CPU.DISP0_DAT17	U24	NVCC_			
J1.53	DISP0_DAT18	CPU.DISP0_DAT18	V25	NVCC_			
J1.55	DISP0_DAT19	CPU.DISP0_DAT19	U23	NVCC_			
J1.57	DISP0_DAT20	CPU.DISP0_DAT20	U22	NVCC_			
J1.59	DISP0_DAT21	CPU.DISP0_DAT21	T20	NVCC_			
J1.61	DGND	DGND	-				
J1.63	DISP0_DAT22	CPU.DISP0_DAT22	V24	NVCC_			

J1 – ODD [1 - 139]							
Pin	***Pin Name***	***Internal Connections***	***Ball/ pin #***	***Supply Group***	***Type***	***Voltage***	***Note***
J1.65	DISP0_DAT23	CPU.DISP0_DAT23	W24	NVCC_			
J1.67	WD_SET0	WDT.SET0	-				
J1.69	WD_SET1	WDT.SET0	-				
J1.71	WD_SET2	WDT.SET0	-				
J1.73	USB_OTG_CHDN	CPU.USB_OTG_CHDN	B8	NVCC_			
J1.75	USB_OTG_VBUS	CPU.USB_OTG_VBUS	E9	NVCC_			
J1.77	USB_OTG_DN	CPU.USB_OTG_DN	B6	NVCC_			
J1.79	USB_OTG_DP	CPU.USB_OTG_DP	A6	NVCC_			
J1.81	DGND	DGND	-				
J1.83	USB_HOST_DP	CPU.USB_HOST_DP	E10	NVCC_			
J1.85	USB_HOST_DN	CPU.USB_HOST_DN	F10	NVCC_			
J1.87	USB_H1_VBUS	CPU.USB_H1_VBUS	D10	NVCC_			
J1.89	SD1_DAT0	CPU.SD1_DAT0	A21	NVCC_			
J1.91	SD1_DAT1	CPU.SD1_DAT1	C20	NVCC_			
J1.93	SD1_DAT2	CPU.SD1_DAT2	E19	NVCC_			
J1.95	SD1_DAT3	CPU.SD1_DAT3	F18	NVCC_			
J1.97	SD1_CMD	CPU.SD1_CMD	B21	NVCC_			
J1.99	SD1_CLK	CPU.SD1_CLK	D20	NVCC_			
J1.101	DGND	DGND	-				
J1.103	SW2_1.8V/3.3V						
J1.105	ETH0_LED1	LAN.LED1/PME_N1	17				
J1.107	ETH0_LED2	LAN.LED2	15				
J1.109	DGND	DGND	-				
J1.111	ETH0_TXRX0_M	LAN.TXRXM_A	3				
J1.113	ETH0_TXRX0_P	LAN.TXRXP_A	2				
J1.115	DGND	DGND	-				
J1.117	ETH0_TXRX1_M	LAN.TXRXM_B	6				
J1.119	ETH0_TXRX1_P	LAN.TXRXP_B	5				
J1.121	DGND	DGND	-				
J1.123	ETH0_TXRX2_M	LAN.TXRXM_C	8				
J1.125	ETH0_TXRX2_P	LAN.TXRXP_C	7				
J1.127	DGND	DGND	-				
J1.129	ETH0_TXRX3_M	LAN.TXRXM_D	11				
J1.131	ETH0_TXRX3_P	LAN.TXRXP_D	10				
J1.133	DGND	DGND	-				
J1.135	RGMII_MDC	CPU.ENET_MDC	V20				
J1.137	RGMII_MDIO	CPU.ENET_MDIO	V23				

J1 – ODD [1 - 139]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J1.139	PMIC_VSNVS	CPU.VDD_SNVS_IN	G11				

J1 – EVEN [2 - 140]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J1.2	LVDS0_TX0_N	CPU.LVDS0_TX0_N	U2				
J1.4	LVDS0_TX0_P	CPU.LVDS0_TX0_P	U1				
J1.6	LVDS0_TX1_N	CPU.LVDS0_TX1_N	U4				
J1.8	LVDS0_TX1_P	CPU.LVDS0_TX1_P	U3				
J1.10	DGND	DGND	-				
J1.12	LVDS0_TX2_N	CPU.LVDS0_TX2_N	V2				
J1.14	LVDS0_TX2_P	CPU.LVDS0_TX2_P	V1				
J1.16	LVDS0_TX3_N	CPU.LVDS0_TX3_N	W2				
J1.18	LVDS0_TX3_P	CPU.LVDS0_TX3_P	W1				
J1.20	LVDS0_CLK_N	CPU.LVDS0_CLK_N	V4				
J1.22	LVDS0_CLK_P	CPU.LVDS0_CLK_P	V3				
J1.24	DGND	DGND	-				
J1.26	CSI0_MCLK	CPU.CSI0_MCLK	P4				
J1.28	DGND	DGND	-				
J1.30	CSI0_PIXCLK	CPU.CSI0_PIXCLK	P1				
J1.32	CSI0_VSYNC	CPU.CSI0_VSYNC	N2				
J1.34	CSI0_DATA_EN	CPU.CSI0_DATA_EN	P3				
J1.36	CSI0_DAT4	CPU.CSI0_DAT4	N1				
J1.38	CSI0_DAT5	CPU.CSI0_DAT5	P2				
J1.40	CSI0_DAT6	CPU.CSI0_DAT6	N4				
J1.42	CSI0_DAT7	CPU.CSI0_DAT7	N3				
J1.44	CSI0_DAT8	CPU.CSI0_DAT8	N6				
J1.46	CSI0_DAT9	CPU.CSI0_DAT9	N5				
J1.48	CSI0_DAT10	CPU.CSI0_DAT10	M1				
J1.50	DGND	DGND	-				
J1.52	CSI0_DAT11	CPU.CSI0_DAT11	M3				
J1.54	CSI0_DAT12	CPU.CSI0_DAT12	M2				
J1.56	CSI0_DAT13	CPU.CSI0_DAT13	L1				
J1.58	CSI0_DAT14	CPU.CSI0_DAT14	M4				

J1 – EVEN [2 - 140]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J1.60	CSI0_DAT15	CPU.CSI0_DAT15	M5				
J1.62	CSI0_DAT16	CPU.CSI0_DAT16	L4				
J1.64	CSI0_DAT17	CPU.CSI0_DAT17	L3				
J1.66	CSI0_DAT18	CPU.CSI0_DAT18	M6				
J1.68	CSI0_DAT19	CPU.CSI0_DAT19	L6				
J1.70	DGND	DGND	-				
J1.72	GPIO_0	CPU.GPIO_0	T5				
J1.74	GPIO_1	CPU.GPIO_1	T4				
J1.76	GPIO_2	CPU.GPIO_2	T1				
J1.78	GPIO_3/I2C3_SCL	CPU.GPIO_3	R7				
J1.80	GPIO_4	CPU.GPIO_4	R6				
J1.82	GPIO_5	CPU.GPIO_5	R4				
J1.84	GPIO_6/I2C3_SDA	CPU.GPIO_6	T3				
J1.86	GPIO_7//FLEXCAN1_H	CPU.GPIO_7	R3				
J1.88	GPIO_8//FLEXCAN1_L	CPU.GPIO_8	R5				
J1.90	DGND	DGND	-				
J1.92	GPIO_9	CPU.GPIO_9	T2				
J1.94	GPIO_16	CPU.GPIO_16	R2				
J1.96	GPIO_17	CPU.GPIO_17	R1				
J1.98	GPIO_18	CPU.GPIO_18	P6				
J1.100	GPIO_19	CPU.GPIO_19	P5				
J1.102	KEY_COL0/ECSPI1_SCLK	CPU.KEY_COL0	W5				
J1.104	KEY_ROW0/ECSPI1_MOSI	CPU.KEY_ROW0	V6				
J1.106	KEY_COL1/ECSPI1_MISO	CPU.KEY_COL1	U7				
J1.108	KEY_ROW1/ECSPI1_SS0	CPU.KEY_ROW1	U6				
J1.110	DGND	DGND	-				
J1.112	KEY_COL2/ECSPI1_SS1	CPU.KEY_COL2	W6				
J1.114	KEY_ROW2	CPU.KEY_ROW2	W4				
J1.116	KEY_COL3/I2C2_SCL	CPU.KEY_COL3	U5				
J1.118	KEY_ROW3/I2C2_SDA	CPU.KEY_ROW3	T7				
J1.120	VGEN4_1V8_I						
J1.122	NVCC_AXEL_I/O_3.3V/1.8V (BOARD_PGOOD)		P7				BOARD_PGOOD signal. Please refer to sections 5.1 and 5.2.
J1.124	RTC_VBAT	RTC.VBAT	6				
J1.126	PMIC_LICELL	PMIC.LICELL	42				
J1.128	SD2_CMD	CPU.SD2_CMD	F19				
J1.130	DGND	DGND	-				

J1 – EVEN [2 - 140]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J1.132	SD2_CLK	CPU.SD2_CLK	C21				
J1.134	SD2_DATA0	CPU.SD2_DATA0	A22				
J1.136	SD2_DATA1	CPU.SD2_DATA1	E20				
J1.138	SD2_DATA2	CPU.SD2_DATA2	A23				
J1.140	SD2_DATA3	CPU.SD2_DATA3	B22				

6.2 Carrier board mating connector J2

J2 – ODD [1-139]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J2.1	DGND	DGND	-				
J2.3	EIM_DA0	CPU.EIM_DA0	L20				
J2.5	EIM_DA1	CPU.EIM_DA1	J25				
J2.7	EIM_DA2	CPU.EIM_DA2	L21				
J2.9	EIM_DA3	CPU.EIM_DA3	K24				
J2.11	EIM_DA4	CPU.EIM_DA4	L22				
J2.13	EIM_DA5	CPU.EIM_DA5	L23				
J2.15	EIM_DA6	CPU.EIM_DA6	K25				
J2.17	EIM_DA7	CPU.EIM_DA7	L25				
J2.19	EIM_DA8	CPU.EIM_DA8	L24				
J2.21	DGND	DGND	-				
J2.23	EIM_DA9	CPU.EIM_DA9	M21				
J2.25	EIM_DA10	CPU.EIM_DA10	M22				
J2.27	EIM_DA11	CPU.EIM_DA11	M20				
J2.29	EIM_DA12	CPU.EIM_DA12	M24				
J2.31	EIM_DA13	CPU.EIM_DA13	M23				
J2.33	EIM_DA14	CPU.EIM_DA14	N23				
J2.35	EIM_DA15	CPU.EIM_DA15	N24				
J2.37	EIM_D16	CPU.EIM_D16	C25				
J2.39	EIM_D17	CPU.EIM_D17	F21				
J2.41	DGND	DGND	-				
J2.43	EIM_D18	CPU.EIM_D18	D24				
J2.45	EIM_D19	CPU.EIM_D19	G21				

J2 – ODD [1-139]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J2.47	EIM_D20	CPU.EIM_D20	G20				
J2.49	EIM_D21	CPU.EIM_D21	H20				
J2.51	EIM_D22	CPU.EIM_D22	E23				
J2.53	EIM_D23	CPU.EIM_D23	D25				
J2.55	EIM_D24	CPU.EIM_D24	F22				
J2.57	EIM_D25	CPU.EIM_D25	G22				
J2.59	EIM_D26	CPU.EIM_D26	E24				
J2.61	DGND	DGND	-				
J2.63	EIM_D27	CPU.EIM_D27	E25				
J2.65	EIM_D28	CPU.EIM_D28	G23				
J2.67	EIM_D29	CPU.EIM_D29	J19				
J2.69	EIM_D30	CPU.EIM_D30	J20				
J2.71	EIM_D31	CPU.EIM_D31	H21				
J2.73	EIM_A16	CPU.EIM_A16	H25				
J2.75	EIM_A17	CPU.EIM_A17	G24				
J2.77	EIM_A18	CPU.EIM_A18	J22				
J2.79	EIM_A19	CPU.EIM_A19	G25				
J2.81	DGND	DGND	-				
J2.83	EIM_A20	CPU.EIM_A20	H22				
J2.85	EIM_A21	CPU.EIM_A21	H23				
J2.87	EIM_A22	CPU.EIM_A22	F24				
J2.89	EIM_A23	CPU.EIM_A23	J21				
J2.91	EIM_A24	CPU.EIM_A24	F25				
J2.93	EIM_A25	CPU.EIM_A25	H19				
J2.95	EIM_LBA	CPU.EIM_LBA	K22				
J2.97	EIM_OE	CPU.EIM_OE	J24				
J2.99	EIM_RW	CPU.EIM_RW	K20				
J2.101	DGND	DGND	-				
J2.103	EIM_BCLK	CPU.EIM_BCLK	N22				
J2.105	EIM_WAIT	CPU.EIM_WAIT	M25				
J2.107	EIM_EB0	CPU.EIM_EB0	K21				
J2.109	EIM_EB1	CPU.EIM_EB1	K23				
J2.111	EIM_EB2	CPU.EIM_EB2	E22				
J2.113	EIM_EB3	CPU.EIM_EB3	F23				
J2.115	EIM_CS0	CPU.EIM_CS0	H24				
J2.117	EIM_CS1	CPU.EIM_CS1	J23				
J2.119	DGND	DGND	-				

J2 – ODD [1-139]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J2.121	PMIC_PROG_VPGM	PMIC.VDDOTP	47				
J2.123	PMIC_PROG_GATE_CTRL		-				
J2.125	2V8-4V5	INPUT VOLTAGE	-				
J2.127	2V8-4V5	INPUT VOLTAGE	-				
J2.129	2V8-4V5	INPUT VOLTAGE	-				
J2.131	2V8-4V5	INPUT VOLTAGE	-				
J2.133	2V8-4V5	INPUT VOLTAGE	-				
J2.135	2V8-4V5	INPUT VOLTAGE	-				
J2.137	2V8-4V5	INPUT VOLTAGE	-				
J2.139	2V8-4V5	INPUT VOLTAGE	-				

J2 – EVEN [2-140]							
Pin	**Pin Name**	**Internal Connections**	**Ball/pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J2.2	NANDF_CS0_B	CPU.NANDF_CS0_B	F15				
J2.4	NANDF_CS1_B	CPU.NANDF_CS1_B	C16				
J2.6	NANDF_CS2_B	CPU.NANDF_CS2_B	A17				
J2.8	NANDF_CS3_B	CPU.NANDF_CS3_B	D16				
J2.10	DGND	DGND	-				
J2.12	NANDF_D0	CPU.NANDF_D0	A18				
J2.14	NANDF_D1	CPU.NANDF_D1	C17				
J2.16	NANDF_D2	CPU.NANDF_D2	F16				
J2.18	NANDF_D3	CPU.NANDF_D3	D17				
J2.20	NANDF_D4	CPU.NANDF_D4	A19				
J2.22	NANDF_D5	CPU.NANDF_D5	B18				
J2.24	NANDF_D6	CPU.NANDF_D6	E17				
J2.26	NANDF_D7	CPU.NANDF_D7	C18				
J2.28	SD4_CLK/NANDF_WE_B	CPU.SD4_CLK	E16				
J2.30	DGND	DGND	-				
J2.32	SD4_DATA0/NANDF_DQS	CPU.SD4_DATA	D18				
J2.34	SD4_CMD/NANDF_RE_B	CPU.SD4_CMD	B17				
J2.36	NANDF_ALE	CPU.NANDF_ALE	A16				
J2.38	NANDF_CLE	CPU.NANDF_CLE	C15				
J2.40	NANDF_WP_B	CPU.NANDF_WP_B	E15				

J2 – EVEN [2-140]							
Pin	**Pin Name**	**Internal Connections**	**Ball/pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J2.42	NANDF_RB0	CPU.NANDF_RB0	B16				
J2.44	SD4_DATA1	CPU.SD4_DATA1	B19				
J2.46	SD4_DATA2	CPU.SD4_DATA2	F17				
J2.48	SD4_DATA3	CPU.SD4_DATA3	A20				
J2.50	DGND	DGND	-				
J2.52	SD4_DATA4	CPU.SD4_DATA4	E18				
J2.54	SD4_DATA5	CPU.SD4_DATA5	C19				
J2.56	SD4_DATA6	CPU.SD4_DATA6	B20				
J2.58	SD4_DATA7	CPU.SD4_DATA7	D19				
J2.60	PMIC_SDWNB	PMIC.SDWNB	2				
J2.62	TEST_MODE	CPU.TEST_MODE	E12				
J2.64	RTC_INTN/SQW	RTC.INT/SQW	3				
J2.66	RTC_RSTN	RTC.RST	4				
J2.68	RTC_32KHZ	RTC.32KHZ	1				
J2.70	DGND	DGND	-				
J2.72	PMIC_INT_B	PMIC.INTB	1				
J2.74	PMIC_PWRON	PMIC.PWRON	56				
J2.76	CPU_ONOFF	CPU.CPU_ONOFF	D12				
J2.78	CPU_PORN	CPU.CPU_PORN	C11				
J2.80	CPU_PMIC_STBY_REQ	CPU.CPU_PMIC_STBY_REQ	F11				
J2.82	CPU_PMIC_ON_REQ	CPU.CPU_PMIC_ON_REQ	D11				
J2.84	BOOT_MODE0	CPU.BOOT_MODE0	C12				
J2.86	BOOT_MODE1	CPU.BOOT_MODE1	F12				
J2.88	MRSTN	MTR.MR	6				
J2.90	DGND	DGND	-				
J2.92	JTAG_TCK	CPU.JTAG_TCK	H5				
J2.94	JTAG_VREF		-				
J2.96	JTAG_TDI	CPU.JTAG_TDI	G5				
J2.98	JTAG_TDO	CPU.JTAG_TDO	G6				
J2.100	JTAG_TMS	CPU.JTAG_TMS	C3				
J2.102	JTAG_NTRST	CPU.JTAG_TRST	C2				
J2.104	NOR_WP	NOR.WP	C4				Pulled-up internally at 3.3V by SPI flash
J2.106	NVCC_CSI_EXT	INTERNAL VOLTAGE SWITCH					Please refer to section 5.1
J2.108	DGND	DGND	-				
J2.110	NVCC_EIM_EXT	INTERNAL VOLTAGE SWITCH					Please refer to section 5.1
J2.112	DGND	DGND	-				
J2.114	NVCC_SD3_EXT	INTERNAL VOLTAGE SWITCH					Please refer to section 5.1

J2 – EVEN [2-140]							
Pin	**Pin Name**	**Internal Connections**	**Ball/pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J2.116	DGND	DGND	-				
J2.118	NVCC_LCD_EXT	INTERNAL VOLTAGE SWITCH					Please refer to section 5.1
J2.120	DGND	DGND	-				
J2.122	PMIC_PROG_SCL		-				
J2.124	PMIC_PROG_SDA		-				
J2.126	2V8-4V5	INPUT VOLTAGE	-				
J2.128	2V8-4V5	INPUT VOLTAGE	-				
J2.130	2V8-4V5	INPUT VOLTAGE	-				
J2.132	2V8-4V5	INPUT VOLTAGE	-				
J2.134	2V8-4V5	INPUT VOLTAGE	-				
J2.136	2V8-4V5	INPUT VOLTAGE	-				
J2.138	2V8-4V5	INPUT VOLTAGE	-				
J2.140	2V8-4V5	INPUT VOLTAGE	-				

6.3 Carrier board mating connector J3

J3 – ODD [1-139]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J3.1	SD3_CLK	CPU.SD3_CLK	D14				
J3.3	DGND	DGND	-				
J3.5	SD3_CMD	CPU.SD3_CMD	B13				
J3.7	SD3_RST	CPU.SD3_RST	D15				
J3.9	DGND	DGND	-				
J3.11	SD3_DATA0	CPU.SD3_DATA0	E14				
J3.13	SD3_DATA1	CPU.SD3_DATA1	F14				
J3.15	SD3_DATA2	CPU.SD3_DATA2	A15				
J3.17	SD3_DATA3	CPU.SD3_DATA3	B15				
J3.19	SD3_DATA4	CPU.SD3_DATA4	D13				
J3.21	SD3_DATA5	CPU.SD3_DATA5	C13				
J3.23	SD3_DATA6	CPU.SD3_DATA6	E13				
J3.25	SD3_DATA7	CPU.SD3_DATA7	F13				
J3.27	DGND	DGND	-				
J3.29	MLB_CN	CPU.MLB_CN	A11				

J3 – ODD [1-139]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J3.31	MLB_CP	CPU.MLB_CP	B11				
J3.33	DGND	DGND	-				
J3.35	MLB_SN	CPU.MLB_SN	A9				
J3.37	MLB_SP	CPU.MLB_SP	B9				
J3.39	DGND	DGND	-				
J3.41	MLB_DN	CPU.MLB_DN	B10				
J3.43	MLB_DP	CPU.MLB_DP	A10				
J3.45	DGND	DGND	-				
J3.47	SATA_RXN	CPU.SATA_RXN	A14				
J3.49	SATA_RXP	CPU.SATA_RXP	B14				
J3.51	DGND	DGND	-				
J3.53	SATA_TXN	CPU.SATA_TXN	B12				
J3.55	SATA_TXP	CPU.SATA_TXP	A12				
J3.57	DGND	DGND	-				
J3.59	CPU_RGMII_TXC_CONN	CPU.RGMII_TXC	D21				
J3.61	DGND	DGND	-				
J3.63	CPU_RGMII_TD0_CONN	CPU.RGMII_TD0	C22				
J3.65	CPU_RGMII_TD1_CONN	CPU.RGMII_TD1	F20				
J3.67	CPU_RGMII_TD2_CONN	CPU.RGMII_TD2	E21				
J3.69	CPU_RGMII_TD3_CONN	CPU.RGMII_TD3	A24				
J3.71	CPU_RGMII_TX_CTL_CONN	CPU.RGMII_TX_CTL	C23				
J3.73	DGND	DGND	-				
J3.75	CPU_RGMII_RXC_CONN	CPU.RGMII_RXC	B25				
J3.77	DGND	DGND	-				
J3.79	CPU_RGMII_RD0_CONN	CPU.RGMII_RD0	C24				
J3.81	CPU_RGMII_RD1_CONN	CPU.RGMII_RD1	B23				
J3.83	CPU_RGMII_RD2_CONN	CPU.RGMII_RD2	B24				
J3.85	CPU_RGMII_RD3_CONN	CPU.RGMII_RD3	D23				
J3.87	CPU_RGMII_RX_CTL_CONN	CPU.RGMII_RX_CTL	D22				
J3.89	DGND	DGND	-				
J3.91	ETH0_CLK125_NDO	LAN.CLK125_NDO	41				
J3.93	DGND	DGND	-				
J3.95	ETH0_INTN	LAN.INT_N/PME_N2	38				
J3.97	ENET_TX_EN/GPIO1_IO28	CPU.ENET_TX_EN	V21				
J3.99	TAMPER	CPU.TAMPER	E11				
J3.101	ENET_REF_CLK//VDDCORE	CPU.ENET_REF_CLK	V22				
J3.103	ENET_RX_ER//VDDSOC	CPU.ENET_RX_ER	W23				

J3 – ODD [1-139]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J3.105	ENET_RXD0//DDR_1V5	CPU.ENET_RXD0	W21				
J3.107	ENET_RXD1	CPU.ENET_RXD1	W22				
J3.109	ENET_TXD0//BB_3.3V/2.5V	CPU.ENET_TXD0	U20				
J3.111	ENET_TXD1//1V2_ETH	CPU.ENET_TXD1	W20				
J3.113	KEY_COL4//ENET_CRS_DV// VDDHIGH_VPH	CPU.KEY_COL4	T6				
J3.115	KEY_ROW4//VDDSOC_CAP	CPU.KEY_ROW4	V5				
J3.117	WDT_WDI//VDDPU	WDT.WDI	1				
J3.119	VDD_ARM23_CAP//VGEN4_1 V8		-				
J3.121	VDD_ARM01_CAP//VGEN5_2 V8//VDD_VBUS_CAP		-				
J3.123	VDD_SNVS_CAP//VGEN3_2V 5//NVCC_PLL_OUT		-				
J3.125	VGEN1		-				
J3.127	VGEN2		-				
J3.129	VGEN6		-				
J3.131	SW4_XV/1.8V		-				
J3.133	PMIC_SWBST_SUPPLY		-				
J3.135	PMIC_SWBST_SUPPLY		-				
J3.137	PMIC_SWBST_SUPPLY		-				
J3.139	DGND	DGND	-				

J3 – EVEN [2-140]							
Pin	**Pin Name**	**Internal Connections**	**Ball/pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J3.2	DGND	DGND	-				
J3.4	CSI_CLK0M	CPU.CSI_CLK0M	F4				
J3.6	CSI_CLK0P	CPU.CSI_CLK0P	F3				
J3.8	DGND	DGND	-				
J3.10	CSI_D0M	CPU.CSI_D0M	E4				
J3.12	CSI_D0P	CPU.CSI_D0P	E3				
J3.14	DGND	DGND	-				
J3.16	CSI_D1M	CPU.CSI_D1M	D1				
J3.18	CSI_D1P	CPU.CSI_D1P	D2				
J3.20	DGND	DGND	-				

J3 – EVEN [2-140]							
Pin	**Pin Name**	**Internal Connections**	**Ball/pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J3.22	CSI_D2M	CPU.CSI_D2M	E1				
J3.24	CSI_D2P	CPU.CSI_D2P	E2				
J3.26	DGND	DGND	-				
J3.28	CSI_D3M	CPU.CSI_D3M	F2				
J3.30	CSI_D3P	CPU.CSI_D3P	F1				
J3.32	DGND	DGND	-				
J3.34	DSI_CLK0M	CPU.DSI_CLK0M	H3				
J3.36	DSI_CLK0P	CPU.DSI_CLK0P	H4				
J3.38	DGND	DGND	-				
J3.40	DSI_D0M	CPU.DSI_D0M	G2				
J3.42	DSI_DOP	CPU.DSI_DOP	G1				
J3.44	DGND	DGND	-				
J3.46	DSI_D1M	CPU.DSI_D1M	H2				
J3.48	DSI_D1P	CPU.DSI_D1P	H1				
J3.50	DGND	DGND	-				
J3.52	LVDS1_TX0_N	CPU.LVDS1_TX0_N	Y1				
J3.54	LVDS1_TX0_P	CPU.LVDS1_TX0_P	Y2				
J3.56	DGND	DGND	-				
J3.58	LVDS1_TX1_N	CPU.LVDS1_TX1_N	AA2				
J3.60	LVDS1_TX1_P	CPU.LVDS1_TX1_P	AA1				
J3.62	DGND	DGND	-				
J3.64	LVDS1_TX2_N	CPU.LVDS1_TX2_N	AB1				
J3.66	LVDS1_TX2_P	CPU.LVDS1_TX2_P	AB2				
J3.68	DGND	DGND	-				
J3.70	LVDS1_CLK_N	CPU.LVDS1_CLK_N	Y3				
J3.72	LVDS1_CLK_P	CPU.LVDS1_CLK_P	Y4				
J3.74	DGND	DGND	-				
J3.76	LVDS1_TX3_N	CPU.LVDS1_TX3_N	AA3				
J3.78	LVDS1_TX3_P	CPU.LVDS1_TX3_P	AA4				
J3.80	DGND	DGND	-				
J3.82	HDMI_CLKN	CPU.HDMI_CLKN	J5				
J3.84	HDMI_CLKP	CPU.HDMI_CLKP	J6				
J3.86	DGND	DGND	-				
J3.88	HDMI_D0N	CPU.HDMI_D0N	K5				
J3.90	HDMI_D0P	CPU.HDMI_D0P	K6				
J3.92	DGND	DGND	-				
J3.94	HDMI_D1N	CPU.HDMI_D1N	J3				

J3 – EVEN [2-140]							
Pin	**Pin Name**	**Internal Connections**	**Ball/pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J3.96	HDMI_D1P	CPU.HDMI_D1P	J4				
J3.98	DGND	DGND	-				
J3.100	HDMI_D2N	CPU.HDMI_D2N	K3				
J3.102	HDMI_D2P	CPU.HDMI_D2P	K4				
J3.104	DGND	DGND	-				
J3.106	HDMI_CEC_IN	CPU.HDMI_DDCCEC	K2				
J3.108	HDMI_HPD	CPU.HDMI_HPD	K1				
J3.110	DGND	DGND	-				
J3.112	CLK1_N	CPU.CLK1_N	C7				
J3.114	CLK1_P	CPU.CLK1_P	D7				
J3.116	DGND	DGND	-				
J3.118	CLK2_N	CPU.CLK2_N	C5				
J3.120	CLK2_P	CPU.CLK2_P	D5				
J3.122	DGND	DGND	-				
J3.124	PCIE_RXN	CPU.PCIE_RXN	B1				
J3.126	PCIE_RXP	CPU.PCIE_RXP	B2				
J3.128	DGND	DGND	-				
J3.130	PCIE_TXN	CPU.PCIE_TXN	A3				
J3.132	PCIE_TXP	CPU.PCIE_TXP	B3				
J3.134	DGND	DGND	-				
J3.136	PMIC_5V		-				
J3.138	PMIC_5V		-				
J3.140	DGND	DGND	-				

7 Peripheral interfaces

AXEL modules implement a number of peripheral interfaces through the J1, J2 and J3 connectors. The following notes apply to those interfaces:

- Some interfaces/signals are available only with/without certain configuration options of the AXEL module. Each signal's availability is noted in the "Notes" column on the table of each interface.
- The peripherals described in the following sections represent the default configuration for the AXEL SOM, which match with the features provided by the electronics implemented on the module.

The signals for each interface are described in the related tables. The following notes summarize the column headers for these tables:

- "Pin name" – The symbolic name of each signal
- "Conn. Pin" – The pin number on the module connectors
- "Function" – Signal description
- "Notes" – This column summarizes configuration requirements and recommendations for each signal.

7.1 Notes on pin assignment

For further information, please refer to section 5.7 "Multiplexing".

7.2 Gigabit Ethernet

On-board Ethernet PHY (Micrel KSZ9031RNX) provides interface signals required to implement the 10/100/1000 Mbps Ethernet port. The transceiver is connected to the triple speed Ethernet MAC (ENET module) through RGMII interface.

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
ETH0_TXRX0_P	J1.113	Media Dependent Interface[0], positive pin	
ETH0_TXRX0_M	J1.111	Media Dependent Interface[0], negative pin	

Pin name	Conn. Pin	Function	Notes
ETH0_TXRX1_P	J1.119	Media Dependent Interface[1], positive pin	
ETH0_TXRX1_M	J1.117	Media Dependent Interface[1], negative pin	
ETH0_TXRX2_P	J1.125	Media Dependent Interface[2], positive pin	
ETH0_TXRX2_M	J1.123	Media Dependent Interface[2], negative pin	
ETH0_TXRX3_P	J1.131	Media Dependent Interface[3], positive pin	
ETH0_TXRX3_M	J1.129	Media Dependent Interface[3], negative pin	
RGMII_MDIO	J1.137	Management Data Input/Output	
RGMII_MDC	J1.135	Management Data Clock input	
ETH0_INTn	J3.95	Interrupt output	
ETH0_LED1	J1.105	Activity LED	
ETH0_LED2	J1.107	Link LED	

7.3 USB

AXEL provides two USB ports with integrated PHY, one USB Host 2.0 (High Speed, up to 480 Mbps) and one USB 2.0 On-The-Go (OTG).

7.3.1 USB Host

Pin name	Conn. Pin	Function	Notes
USB_HOST_DP	J1.83	D+ pin of the USB cable	
USB_HOST_DN	J1.85	D- pin of the USB cable	
USB_H1_VBUS	J1.87	VBUS pin of the USB cable	

7.3.2 USB OTG

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
USB_OTG_DN	J1.77	D- pin of the USB cable	
USB_OTG_DP	J1.79	D+ pin of the USB cable	
USB_OTG_VBUS	J1.75	VBUS pin of the USB cable	
USB_OTG_ID	J2.113 J1.74	USB OTG ID	
USB_OTG_CHDn	J1.73	Charge detect signal	

7.4 Video Output ports

i.MX6 implements two (identical) Image Processing Units (IPUs), which provide connectivity to displays and related processing, synchronization and control. Each IPU has two display ports - each controlled by a DI module - providing a connection to displays and external devices, either directly (parallel interface) or via bridges (MIPI, LVDS, HDMI). Each IPU has 2 display ports, up to four external ports can be active at any given time. (Additional asynchronous data flows can be sent though the parallel ports and the MIPI/DSI port.). The following is a list of the available interfaces:

- Two parallel ports, driven directly by each of the IPUs
- Two LVDS channels, driven by the LDB
- One HDMI port (ver. 1.4), driven by the HDMI transmitter
- One MIPI/DSI port, driven by the MIPI/DSI transmitter; 2 data lanes at 1 GHz

Each IPU display port (DI) can be connected to each of the above ports.

7.4.1 LVDS

The LVDS Display Bridge (LDB) connects the IPU (Image Processing Unit) to an External LVDS Display Interface. There are 2 LVDS channels. These outputs are used to communicate RGB data and controls to external LCD displays.
The LVDS ports may be used as follows:

- Single channel output
- Dual channel output (one input source, two channels outputs for two

displays)

- Split channel output (one input source, splitted to 2 channels on output)
- Separate 2 channel output (2 input sources from IPU).

The output LVDS port complies to the EIA-644-A standard.

7.4.1.1 LVDS0

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
LVDS0_DATA[0]_N	J1.2	LVDS0 negative data 0 signal	
LVDS0_DATA[0]_P	J1.4	LVDS0 positive data 0 signal	
LVDS0_DATA[1]_N	J1.6	LVDS0 negative data 1 signal	
LVDS0_DATA[1]_P	J1.8	LVDS0 positive data 1 signal	
LVDS0_DATA[2]_N	J1.12	LVDS0 negative data 2 signal	
LVDS0_DATA[2]_P	J1.14	LVDS0 positive data 2 signal	
LVDS0_DATA[3]_N	J1.16	LVDS0 negative data 2 signal	
LVDS0_DATA[3]_P	J1.18	LVDS0 positive data 2 signal	
LVDS0_CLK_N	J1.20	LVDS0 negative clock signal	
LVDS0_CLK_P	J1.22	LVDS0 positive clock signal	

7.4.1.2 LVDS1

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
LVDS1_TX0_N	J3.52	LVDS1 negative data 0 signal	
LVDS1_TX0_P	J3.54	LVDS1 positive data 0	

Pin name	Conn. Pin	Function	Notes
		signal	
LVDS1_TX1_N	J3.58	LVDS1 negative data 1 signal	
LVDS1_TX1_P	J3.60	LVDS1 positive data 1 signal	
LVDS1_TX2_N	J3.64	LVDS1 negative data 2 signal	
LVDS1_TX2_P	J3.66	LVDS1 positive data 2 signal	
LVDS1_TX3_N	J3.76	LVDS1 negative data 3 signal	
LVDS1_TX3_P	J3.78	LVDS1 positive data 3 signal	
LVDS1_CLK_N	J3.70	LVDS1 negative clock signal	
LVDS1_CLK_P	J3.72	LVDS1 positive clock signal	

7.4.2 HDMI

The HDMI interface available on AXEL is based on the HDMI transmitter and the HDMI 3D Tx PHY integrated into the i.MX6 SoC. The HDMI port supports the following standards and features:

- High-Definition Multimedia Interface Specification, Version 1.4a
- Support for up to 1080p at 60Hz HDTV display resolutions and up to QXGA graphic display resolutions.
- Support for 4k x 2k and 3D video formats
- Support for up to 16-bit Deep Color modes

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
HDMI_TX_CLK_N	J3.82	HDMI negative clock signal	
HDMI_TX_CLK_P	J3.84	HDMI positive clock signal	

Pin name	Conn. Pin	Function	Notes
HDMI_TX_DATA0_N	J3.88	HDMI negative data 0	
HDMI_TX_DATA0_P	J3.90	HDMI positive data 0	
HDMI_TX_DATA1_N	J3.94	HDMI negative data 1	
HDMI_TX_DATA1_P	J3.96	HDMI positive data 1	
HDMI_TX_DATA2_N	J3.100	HDMI negative data 2	
HDMI_TX_DATA2_P	J3.102	HDMI positive data 2	
HDMI_TX_DDC_CEC	J3.106	HDMI CEC signal	
HDMI_TX_DDC_SCL	J1.116 J2.111	HDMI I2C clock signal	
HDMI_TX_DDC_SDA	J1.118 J2.37	HDMI I2C data signal	
HDMI_TX_HPD	J3.108	HDMI HPD signal	

7.4.3 Parallel RGB

The Parallel Display interface provided by AXEL is derived directly from the DI0 port of the IPU, bypassing all the i.MX6 integrated display bridges.
The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
DI0_DISP_CLK	J1.3	Pixel clock	
DI0_PIN2	J1.5	Horizontal synchronization	
DI0_PIN3	J1.7	Vertical synchronization	
DI0_PIN15	J1.11	Data valid/blank, data enable	
DISP0_DAT0	J1.13	Pixel data bit 0	
DISP0_DAT1	J1.15	Pixel data bit 1	
DISP0_DAT2	J1.17	Pixel data bit 2	
DISP0_DAT3	J1.19	Pixel data bit 3	
DISP0_DAT4	J1.23	Pixel data bit 4	
DISP0_DAT5	J1.25	Pixel data bit 5	
DISP0_DAT6	J1.27	Pixel data bit 6	

Pin name	Conn. Pin	Function	Notes
DISP0_DAT7	J1.29	Pixel data bit 7	
DISP0_DAT8	J1.31	Pixel data bit 8	
DISP0_DAT9	J1.33	Pixel data bit 9	
DISP0_DAT10	J1.35	Pixel data bit 10	
DISP0_DAT11	J1.37	Pixel data bit 11	
DISP0_DAT12	J1.39	Pixel data bit 12	
DISP0_DAT13	J1.43	Pixel data bit 13	
DISP0_DAT14	J1.45	Pixel data bit 14	
DISP0_DAT15	J1.47	Pixel data bit 15	
DISP0_DAT16	J1.49	Pixel data bit 16	
DISP0_DAT17	J1.51	Pixel data bit 17	
DISP0_DAT18	J1.53	Pixel data bit 18	
DISP0_DAT19	J1.55	Pixel data bit 19	
DISP0_DAT20	J1.57	Pixel data bit 20	
DISP0_DAT21	J1.59	Pixel data bit 21	
DISP0_DAT22	J1.63	Pixel data bit 22	
DISP0_DAT23	J1.65	Pixel data bit 23	

7.4.4 MIPI DSI

AXEL provides the MIPI Display interface derived from the i.MX6 integrated MIPI-DSI host controller, which acts as a bridge between the IPU and the MIPI D-PHY, enabling the communication with a MIPI-DSI compliant display through up to two D-PHY Data Lanes.

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
DSI_CLK0M	J3.34	MIPI Display Differential clock pair	
DSI_CLK0P	J3.36		
DSI_D0M	J3.40	MIPI Display Differential data 0 pair	
DSI_D0P	J3.42		
DSI_D1M	J3.46	MIPI Display Differential	

Pin name	Conn. Pin	Function	Notes
DSI_D1P	J3.458	data 1 pair	

7.5 Video Input ports

This section will be completed in a future version of this manual.

7.5.1 Parallel RGB

This section will be completed in a future version of this manual.

7.5.2 MIPI CSI

This section will be completed in a future version of this manual.

7.6 UARTs

Five UART ports are routed to AXEL connectors. UART1 provides full Modem Control Signals, while UART2, UART3, UART4 and UART5 are 4-wire interfaces. Each port can be programmed separately (also in IrDA mode).

7.6.1 UART1

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Note
UART1_CTS	J2.45 J3.11	Clear to send	
UART1_DCD	J2.53	Data carrier detected	
UART1_DSR	J2.57	Data set ready	
UART1_DTR	J2.55	Data terminal ready	
UART1_RI	J2.113	Ring indicator	
UART1_RTS	J2.47 J3.13	Request to send	
UART1_RX_DATA	J1.52 J3.23	Serial/infrared data receive	
UART1_TX_DATA	J1.48 J3.25	Serial/infrared data transmit	

7.6.2 UART2

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
UART2_CTS	J2.65 J3.5 J2.56	Clear to send	
UART2_RTS	J2.67 J3.1 J2.54	Request to send	
UART2_RX_DATA	J2.63 J1.88 J3.19 J2.52	Serial/infrared data receive	
UART2_TX_DATA	J2.59 J1.86 J3.21 J2.58	Serial/infrared data transmit	

7.6.3 UART3

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
UART3_CTS	J2.53 J2.69 J3.17	Clear to send	
UART3_RTS	J2.71 J2.113 J3.7	Request to send	
UART3_RX_DATA	J2.57 J2.28	Serial/infrared data receive	
UART3_TX_DATA	J2.55 J2.34	Serial/infrared data transmit	

7.6.4 UART4

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
UART4_CTS	J1.64	Clear to send	
UART4_RTS	J1.62	Request to send	
UART4_RX_DATA	J1.56 J1.104	Serial/infrared data receive	
UART4_TX_DATA	J1.54 J1.102	Serial/infrared data transmit	

7.6.5 UART5

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
UART5_CTS	J1.68 J3.115	Clear to send	
UART5_RTS	J1.66 J3.113	Request to send	
UART5_RX_DATA	J1.60 J1.108	Serial/infrared data receive	
UART5_TX_DATA	J1.58 J1.106	Serial/infrared data transmit	

7.7 SPI

AXEL provides five SPI ports connected to the I.MX6 integrated Enhanced Configurable SPI (ECSPI) controller, featuring:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Up to four Chip Select (SS) signals to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- Configurable Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK)
- Direct Memory Access (DMA) support

7.7.1 ECSPI1

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
ECSPI1_MISO	J1.106 J1.40 J1.63 J2.39	Master data in; slave data out	
ECSPI1_MOSI	J1.104 J1.38 J1.59 J2.43	Master data out; slave data in	
ECSPI1_RDY	J1.100	Data ready signal	
ECSPI1_SCLK	J1.102 J1.36 J1.57 J2.37	Clock signal	
ECSPI1_SS0	J1.108 J1.42 J1.65 J2.111	Chip select 0 signal	
ECSPI1_SS1	J1.112 J1.47 J2.45	Chip select 1 signal	
ECSPI1_SS2	J1.114 J2.55	Chip select 2 signal	
ECSPI1_SS3	J1.116 J2.57	Chip select 3 signal	

7.7.2 ECSPI2

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
ECSPI2_MISO	J1.48 J1.51 J2.97	Master data in; slave data out	
ECSPI2_MOSI	J1.46 J1.49 J2.117	Master data out; slave data in	

Pin name	Conn. Pin	Function	Notes
ECSPI2_RDY	J2.93	Data ready signal	
ECSPI2_SCLK	J1.44 J1.55 J2.115	Clock signal	
ECSPI2_SS0	J1.52 J1.53 J2.99	Chip select 0 signal	
ECSPI2_SS1	J1.47 J2.95	Chip select 1 signal	
ECSPI2_SS2	J2.55	Chip select 2 signal	
ECSPI2_SS3	J2.57	Chip select 3 signal	

7.7.3 ECSPI3

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
ECSPI3_MISO	J1.17	Master data in; slave data out	
ECSPI3_MOSI	J1.15	Master data out; slave data in	
ECSPI3_RDY	J1.29	Data ready signal	
ECSPI3_SCLK	J1.13	Clock signal	
ECSPI3_SS0	J1.19	Chip select 0 signal	
ECSPI3_SS1	J1.23	Chip select 1 signal	
ECSPI3_SS2	J1.25	Chip select 2 signal	
ECSPI3_SS3	J1.27	Chip select 3 signal	

7.7.4 ECSPI4

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
ECSPI4_MISO	J2.51	Master data in; slave data out	

Pin name	Conn. Pin	Function	Notes
ECSPI4_MOSI	J2.65	Master data out; slave data in	
ECSPI4_RDY	J2.113	Data ready signal	
ECSPI4_SCLK	J2.49	Clock signal	
ECSPI4_SS0	J2.47 J2.67	Chip select 0 signal	
ECSPI4_SS1	J2.93	Chip select 1 signal	
ECSPI4_SS2	J2.55	Chip select 2 signal	
ECSPI4_SS3	J2.57	Chip select 3 signal	

7.7.5 ECSPI5

AXEL on-board bootable SPI Flash is interfaced with the i.MX6 SoC through the eCSPI5 port on chip select 0.

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
ECSPI5_MISO	J1.89 J1.134	Master data in; slave data out	
ECSPI5_MOSI	J1.97 J1.128	Master data out; slave data in	
ECSPI5_RDY	J1.86	Data ready signal	
ECSPI5_SCLK	J1.99 J1.132	Clock signal	
ECSPI5_SS0	J1.91 J1.136	Chip select 0 signal	
ECSPI5_SS1	J1.93 J1.138	Chip select 1 signal	
ECSPI5_SS2	J1.95	Chip select 2 signal	
ECSPI5_SS3	J1.140	Chip select 3 signal	

7.8 Raw NAND flash controller

Raw NAND flash memory controller signals are routed to the connectors to connect an external flash NAND memory chip.

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
NAND_ALE	J2.36	Address latch enable signal	
NAND_CE0_B	J2.2	Chip enable 0 signal	
NAND_CE1_B	J2.4	Chip enable 1 signal	
NAND_CE2_B	J2.6	Chip enable 2 signal	
NAND_CE3_B	J2.8	Chip enable 3 signal	
NAND_CLE	J2.38	Command latch enable signal	
NAND_DATAO0	J2.12	Data signal 0	
NAND_DATAO1	J2.14	Data signal 1	
NAND_DATAO2	J2.16	Data signal 2	
NAND_DATAO3	J2.18	Data signal 3	
NAND_DATAO4	J2.20	Data signal 4	
NAND_DATAO5	J2.22	Data signal 5	
NAND_DATAO6	J2.24	Data signal 6	
NAND_DATAO7	J2.26	Data signal 7	
NAND_DQS	J2.32	DQS signal	
NAND_READY_B	J2.42	Ready signal	
NAND_RE_B	J2.34	Read enable signal	
NAND_WE_B	J2.28	Write enable signal	
NAND_WP_B	J2.40	Wait polarity signal	

7.9 I²C

Three I²C channels are available on AXEL to provide an interface to other devices compliant with Philips Semiconductors Inter-IC bus (I2C-bus™) specification version 2.1. The I²C ports support standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s).

7.9.1 I²C1

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
I2C1_SCL	J1.46 J2.49	I2C clock	
I2C1_SDA	J1.44 J2.65	I2C data	

7.9.2 I²C2

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
I2C2_SCL	J1.116 J2.111	I2C clock	
I2C2_SDA	J1.118 J2.37	I2C data	

7.9.3 I²C3

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
I2C3_SCL	J1.78 J2.39 J1.82	I2C clock	
I2C3_SDA	J1.84 J2.43 J1.94	I2C data	

7.10 CAN

AXEL provides two CAN interfaces (FLEXCAN1 and FLEXCAN2) for supporting distributed realtime control with a high level of reliability. The FLEXCAN module implements the CAN protocol version 2.0 part B and supports bit rates up to 1 Mbit/s.

7.10.1 FLEXCAN1

FLEXCAN1 port is connected to on-board transceiver (TI SN65HVD232) which converts the single-ended CAN signals of the controller to the differential signals of the physical layer. When required, the on-board

transceiver can be excluded by dedicated mount options. Please contact our Sales Department for more information about this hardware option.

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
CAN_H	J1.86	High bus output	
CAN_L	J1.88	Low bus output	

The following table describes FLEXCAN1 interface signals:

Pin name	Conn. Pin	Function	Notes
FLEXCAN1_RX	J1.88 J1.114 J3.1	Receive data pin	
FLEXCAN1_TX	J1.86 J1.112 J3.5	Transmit data pin	

7.10.2 FLEXCAN2

When required, FLEXCAN2 must be connected to an external PHY on the carrier board.

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
FLEXCAN2_RX	J3.115 J3.13	Receive data pin	
FLEXCAN2_TX	J3.113 J3.11	Transmit data pin	

7.11 JTAG

The i.MX6 provides debug access via a standard JTAG (IEEE 1149.1) debug interface.

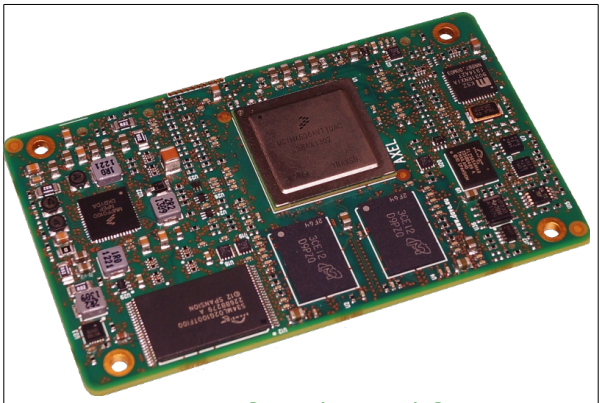


Fig. 6: AXEL – Solo / Dual / Quad core ARM Cortex A9

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
JTAG_TDO	J2.98	JTAG TDO	
JTAG_TDI	J2.96	JTAG TDI	
JTAG_TMS	J2.100	JTAG TMS	
JTAG_TCK	J2.92	JTAG clock	
JTAG_VREF	J2.94	JTAG VREF	
JTAG_nTRST	J2.102	JTAG TRST	

7.12 SD/SDIO/MMC

Four standard MMC/SD/SDIO interfaces are available on AXEL SOM. The processor provides 4 MMC/SD/SDIO ports through the ULTRA Secured Digital Host Controller (USDHC), compliant with MMC V4.41, Secure Digital Memory Card Specification V3.00 and Secure Digital Input Output (SDIO) V3.00 specifications. The controller supports 1-bit / 4-bit

SD and SDIO modes, 1-bit / 4-bit / 8-bit MMC modes. High capacity SD cards (SDHC) are supported.

7.12.1 MMC/SD/SDIO1

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
SD1_CD	J1.74	Card detection pin	If not used(for the embedded memory),tie low to indicate there is a card attached.
SD1_CLK	J1.99	Clock for MMC/SD/SDIO card	
SD1_CMD	J1.97	CMD line	
SD1_DATA0	J1.89	DATA0 line in all modes	Also used to detect busy state
SD1_DATA1	J1.91	DATA1 line in 4/8-bit mode	Also used to detect interrupt in 1/4-bit mode
SD1_DATA2	J1.93	DATA2 line or Read Wait in 4-bit mode	Read Wait in 1-bit mode
SD1_DATA3	J1.95	DATA3 line in 4/8-bit mode or configured as card detection pin	May be configured as card detection pin in 1-bit mode
SD1_DATA4	J2.12	DATA4 line in 8-bit mode, not used in other modes	
SD1_DATA5	J2.14	DATA5 line in 8-bit mode, not used in other modes	
SD1_DATA6	J2.16	DATA6 line in 8-bit mode, not used in other modes	
SD1_DATA7	J2.18	DATA7 line in 8-bit mode, not used in other modes	
SD1_LCTL	J1.94	LED control used to drive an	Fully controlled by the driver

Pin name	Conn. Pin	Function	Notes
		external LED Active high	Optional output
SD1_VSELECT	J1.106 J1.116	IO power voltage selection signal	
SD1_WP	J1.9 J1.92	Card write protect detect	If not used(for the embedded memory), tie low to indicate it's not write protected.

7.12.2 MMC/SD/SDIO2

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
SD2_CD	J1.80	Card detection pin	If not used(for the embedded memory),tie low to indicate there is a card attached.
SD2_CLK	J1.132	Clock for MMC/SD/SDIO card	
SD2_CMD	J1.128	CMD line	
SD2_DATA0	J1.134	DATA0 line in all modes	Also used to detect busy state
SD2_DATA1	J1.136	DATA1 line in 4/8-bit mode	Also used to detect interrupt in 1/4-bit mode
SD2_DATA2	J1.138	DATA2 line or Read Wait in 4-bit mode	Read Wait in 1-bit mode
SD2_DATA3	J1.140	DATA3 line in 4/8-bit mode or configured as card detection pin	May be configured as card detection pin in 1-bit mode
SD2_DATA4	J2.20	DATA4 line in 8-bit mode, not used in other modes	
SD2_DATA5	J2.22	DATA5 line in 8-bit	

Pin name	Conn. Pin	Function	Notes
		mode, not used in other modes	
SD2_DATA6	J2.24	DATA6 line in 8-bit mode, not used in other modes	
SD2_DATA7	J2.26	DATA7 line in 8-bit mode, not used in other modes	
SD2_LCTL	J1.84	LED control used to drive an external LED Active high	Fully controlled by the driver Optional output
SD2_VSELECT	J1.108 J1.114	IO power voltage selection signal	
SD2_WP	J1.76	Card write protect detect	If not used(for the embedded memory), tie low to indicate it's not write protected.

7.12.3 MMC/SD/SDIO3

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
SD3_CLK	J3.1	Clock for MMC/SD/SDIO card	
SD3_CMD	J3.5	CMD line	
SD3_DATA0	J3.11	DATA0 line in all modes	Also used to detect busy state
SD3_DATA1	J3.13	DATA1 line in 4/8-bit mode	Also used to detect interrupt in 1/4-bit mode
SD3_DATA2	J3.15	DATA2 line or Read Wait in 4-bit mode	Read Wait in 1-bit mode
SD3_DATA3	J3.17	DATA3 line in 4/8-bit mode or configured as card	May be configured as card detection pin in 1-bit mode

Pin name	Conn. Pin	Function	Notes
		detection pin	
SD3_DATA4	J3.19	DATA4 line in 8-bit mode, not used in other modes	
SD3_DATA5	J3.21	DATA5 line in 8-bit mode, not used in other modes	
SD3_DATA6	J3.23	DATA6 line in 8-bit mode, not used in other modes	
SD3_DATA7	J3.25	DATA7 line in 8-bit mode, not used in other modes	
SD3_RESET	J3.7	Card hardware reset signal, active LOW	
SD3_VSELECT	J1.98 J2.4	IO power voltage selection signal	

7.12.4 MMC/SD/SDIO4

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
SD4_CLK	J2.28	Clock for MMC/SD/SDIO card	
SD4_CMD	J2.34	CMD line	
SD4_DATA0	J2.32	DATA0 line in all modes	Also used to detect busy state
SD4_DATA1	J2.44	DATA1 line in 4/8-bit mode	Also used to detect interrupt in 1/4-bit mode
SD4_DATA2	J2.46	DATA2 line or Read Wait in 4-bit mode	Read Wait in 1-bit mode
SD4_DATA3	J2.48	DATA3 line in 4/8-bit mode or configured as card detection pin	May be configured as card detection pin in 1-bit mode

Pin name	Conn. Pin	Function	Notes
SD4_DATA4	J2.52	DATA4 line in 8-bit mode, not used in other modes	
SD4_DATA5	J2.54	DATA5 line in 8-bit mode, not used in other modes	
SD4_DATA6	J2.56	DATA6 line in 8-bit mode, not used in other modes	
SD4_DATA7	J2.58	DATA7 line in 8-bit mode, not used in other modes	
SD4_RESET	J2.36	Card hardware reset signal, active LOW	
SD4_VSELECT	J2.4	IO power voltage selection signal	

7.13 PCI Express

The SOM supports connections to PCIe-compliant devices via the integrated PCIe master/slave bus interface. The i.MX6 integrated PCIe module implements a single one-lane PCIe 2.0 (5.0 GT/s) Dual Mode/Endpoint/Root Complex port.

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
PCIE_TXM	J3.130	PCIE Transmit Data Lane 0	
PCIE_TXP	J3.132		
PCIE_RXM	J3.124	PCIE Receive Data Lane 0.	
PCIE_RXP	J3.126		

7.14 SATA

AXEL provides a Serial ATA-II (SATA-II) 3.0 Gbps controller with integrated PHY, which supports all SATA power management features, eSATA and hardware-assisted native command queuing (NCQ) for up to

32 entries.

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
SATA_TXM	J3.53	Serial ATA data transmit	
SATA_TXP	J3.55		
SATA_RXM	J3.47	Serial ATA data receive	
SATA_RXP	J3.49		

7.15 Audio interface

This section will be completed in a future version of this manual.

7.16 Keypad

This section will be completed in a future version of this manual.

7.17 GPIO

The i.MX6 GPIO module provides general-purpose pins that can be configured as either inputs or outputs, for connections to external devices. In addition, the GPIO peripheral can produce CORE interrupts. The device contains eight GPIO blocks and each GPIO block is made up of 32 identical channels.
The device GPIO peripheral supports up to 256 3.3-V GPIO pins. Each channel must be properly configured, since GPIO signals are multiplexed with other interfaces signals. For more information on how to configure and use GPIOs, please refer to section 5.7. For additional details, please refer to section 27 of the i.MX 6 APRM.

8 Operational characteristics

8.1 Maximum ratings

This section will be completed in a future version of this manual.

Parameter	Min	Typ	Max	Unit
Main power supply voltage	2.8	3.3	4.5	V

8.2 Recommended ratings

This section will be completed in a future version of this manual.

Parameter	Min	Typ	Max	Unit
Main power supply voltage	2.8	3.3	4.5	V

8.3 Power consumption

Providing theoretical maximum power consumption value would be useless for the majority of system designers building their application upon AXEL module because, in most cases, this would lead to an over-sized power supply unit.
Several configurations have been tested in order to provide figures that are measured on real-world use cases instead. Please note that AXEL platform is so flexible that it is virtually impossible to test for all possible configurations and applications on the market. The use cases here presented should cover most of real-world scenarios. However actual customer application might require more power than values reported here. Generally speaking, application specific requirements have to be taken into consideration in order to size power supply unit and to implement thermal management properly.

8.3.1 Set 1

This section will be completed in a future version of this manual.

8.3.2 Set 2

This section will be completed in a future version of this manual.

8.4 Heat Dissipation

Qualification of the microprocessors has been deeply changed with respect to some years ago. Silicon manufactures today qualify ICs measuring the temperature at dye level, that is conceptually correct since we are dealing with silicon. On the other hand, users are loosing the straightforward relationship with the “ambient temperature”, that is the end- user parameter still popular and evaluated when they must choose a platform for their needs.

Therefore, a deep knowledge of the heat transfer mechanism from junction to environment is absolutely needed. Also, to know how to save power consumption and to dissipate heating is of primary importance.

Application Note AN4579[2] released by Freescale/NXP is a fundamental guide in understanding thermal dissipation of iMX6 components.
We strongly recommend to read, understand, and follow all suggestions described in that guide.

AN4579 deals with the twofold aspects of the problem. The first aspect is related to the power saving strategy to be implemented. That are implemented in software on an hardware properly set.
DAVE Embedded Systems has implemented in the Linux BSP, and maintained in the time, many of the Software Thermal Management Techniques listed in the Application Notes. Check with your DAVE Embedded Systems' Technical Support which are currently maintained and which are the default settings.

Once power has been managed at best as mentioned above, heat dissipation is also to be managed. Starting from the standard consumption described in the “use cases” above [see also AN4576[3], AN4509[4] and AN4715[5] and http://wiki.dave.eu/index.php/Power_consumption_(AxelLite)] , using fundamental formula

$$T_j = T_a + R_{ja} * P$$

and knowing that R_{ja} =22 °C/W for no-lid i.MX6 case, you can verify that

2 AN4579: Thermal Management Guidelines
3 AN4576: i.MX6 DualLite Power Consumption Measurement
4 AN4509: i.MX6 Dual/Quad Power Consumption Measurement
5 AN4715: i.MX6 Solo Consumption Measurement

natural convection with no heat sink make CPU working only around 20-25°C (see table 10)
To lower R_{ja} - the only available parameter – you must use of a (passive) heatsink in such a way you can dissipate same power at a considerably high ambient temperature. If you add an air flow on the heatsink you can dissipate at an even higher temperature.
The following table shows an example, on how much power can be dissipated with T_j =105°C and T_a =25°C without heatsink/still air (a), with heatsink*/still air (b), with heatsink/air flow 1m/s (c), with heatsink/air flow 4m/s (d):

Use Case	T_j	T_a	R_{ja}	P [W]
a	105°C	25°C	22	3,64
b	105°C	25°C	12,9	6,20
c	105°C	25°C	6,9 (1m/s)	11,60
d	105°C	25°C	4,5 (4m/s)	17,78

Tab. 10: Power dissipation Vs.Thermal Resistance

The following table shows the T_a the system can work at, in the same "use case" when the CPU is supposed to consume 4W

Use Case	T_j	T_a	R_{ja}	P [W]
a	105°C	25°C	22	4
b	105°C	53°C	12,9	4
c	105°C	77°C	6,9 (1m/s)	4
d	105°C	87°C	4,5 (4m/s)	4

Tab. 11: Ambient Temperature Vs.Thermal Resistance

It is mandatory to understand that Thermal Management Techniques are under the responsability of the system integrator. Even if these notes try to help also with some quantitative suggestion, every solution must be validated by the System Integrator itself at the end of the integration process. That is due to the fact that too many parameters that are affecting simulations are

not taken in account because it very difficult to modelize them. Therefore, even if customers may afford these kind of design, the simulation itself would be affected by huge uncertainty.

9 Application notes

Please refer to the following documents available on **DAVE Embedded Systems** Developers Wiki:

Document	Location
Integration Guide	http://wiki.dave.eu/index.php/Integration_guide_%28Axel%29
Carrier board design guidelines	http://wiki.dave.eu/index.php/Carrier_board_design_guidelines_%28SOM%29